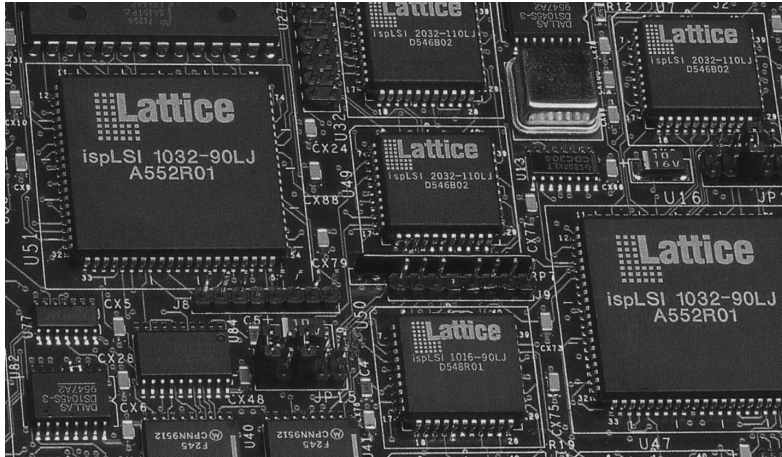


4200 Series Testing ISP Devices



Enables the programming of ISP devices to increase the functionality of the test system

- On-board device programming and verification
- Handles single or multiple devices
- Fully integrated into in-circuit test program
- No additional 4200 hardware required
- Supports popular ISP devices e.g Lattice 1000 and 2000 Series, xilinx XC9500 Series

Introduction

ISP, or In Situ programmable devices can be programmed, erased and then re-programmed. This allows special test code to be used during the manufacturing process to simplify test.

The 4200 ISP programming option allows the 4200 series manufacturing test systems to program and verify these devices as part of a normal in-circuit test.

By using the 4200 series of testers to perform the production programming of ISP devices, it eliminates the need for stand-alone device programming stations. This provides a great saving in terms of both time and money.

The programming code can be produced for a single ISP device or a daisy chain of ISP devices. To achieve this the software requires a JEDEC file describing the configuration of the device.

A programming vector file is produced via the appropriate vector generation software, for example Lattice's ispVM and Xilinx's IMPACT. This generic vector file can then be converted into a format required for the 4200 series of testers.

The Computer Aided Program Generation software (CAPG) is used to create an In-Circuit test program which contains all the necessary converted ISP programming code.

CAPG may be run either on the test system or on any other supported platform.

System Requirements

The ISP programming option for the 4200 series of testers is a software only option and hence is very simple and cost effective to implement.

No extra hardware is needed for the implementation of this option as the 4200 has all the required hardware already as standard on the system.

4200 Series ISP Software

To create a test for Lattice ISP devices there are two main stages to follow.

The first is to create a generic vector file using ispVM. The input files required for this process are a JEDEC file (describing the fuse map information for the particular device) and also a .DLD file which describes an ISP chain, including the order of the devices in the chain. The generic vector file produced from the ispVM software is then used as the input for the second stage.

This generic file is in ASCII format and needs to be converted into a binary format suitable for programming ispLSI devices during the testing of a PCB. The generic vector file goes through two convert-

ers, firstly avgen which converts the ASCII generic file into an ASCII file in an Aeroflex format. This file is then converted using bvgen which converts the file into a binary format ready to use during board test.

For Xilinx devices the process is similar except that an SVF file is created using the Xilinx IMPACT tool. The SVF file is then processed with CAPG to create the binary .buf file.

CAPG is used in the normal way to generate the test program for the board. A MTL library module is provided which is used to control the state machine of the device. This module is included into the test program by CAPG and uses the data from the binary data file to program and verify the devices.

At runtime the binary programming data is loaded into the 4200 series pattern generators and this is used to shift the data into the device chain. Any errors in programming (such as a verification failure) will be reported by the existing software in the usual way.

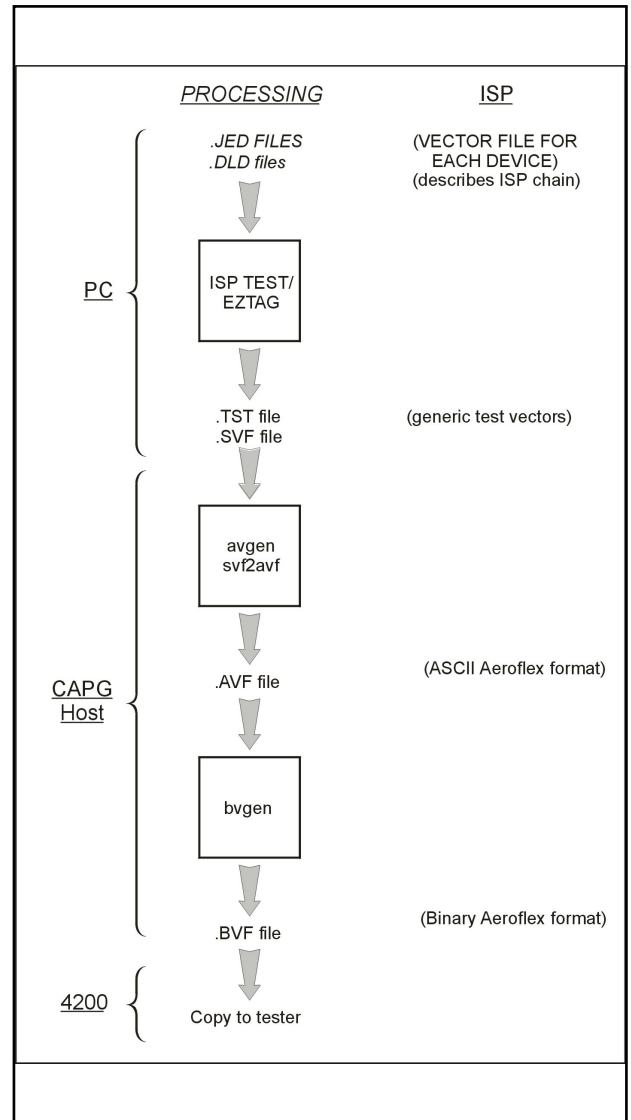
Results may also be logged in the usual way to the Test Area Management system, i-Base, as this option is fully supported.

Test Strategy

Whilst programming the ispLSI device is reduced to a simple task by the use of this software, testing a correctly programmed device can be more of a complicated procedure, depending on the device's functionality.

Therefore, to greatly simplify the testing of these devices, a two stage test strategy would be used thus increasing board level quality and reliability.

The device would first be configured as a simple series of digital gates or in a Nand Tree structure. These devices would then be tested along with the other digital devices on the board. If the In-Circuit test proves successful, they would be re-programmed using the final functional design data to complete the board test.



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