

UTMC PRODUCT ADVISORY

UT22VP10 RADPAL Power-On-Reset Ramp Rate Anomaly

UTMC has identified the following anomaly in the power up behavior of the UT22VP10 RAD_{PAL} (RC01 and RC02).

Anomaly:

The anomaly was observed for a power-up application where a residual voltage between 200 and 500 mV was supplied to the V_{DD} pin(s) of the RAD_{PAL} for several milliseconds prior to the 5V power supply ramping to 5 volts. Consequently, the RAD_{PAL} enters a “test” mode (as opposed to a “user” mode). In the test mode, all output buffers are placed and remain in a high impedance state and the RAD_{PAL} does not function as programmed.

Through HSPICE simulation and laboratory tests, UTMC has found there exists a window in which a residual voltage of a few hundred millivolts on the V_{DD} pin(s) prevents the RAD_{PAL} from generating an internal POR signal for its security circuit. The lack of a reset signal allows the security circuit to power up in either the “user” or the “test” mode of operation. Entering the “test” mode prevents the RAD_{PAL} from functioning as programmed. The anomaly is seen at room temperature and above, where a residual voltage above 200mV is applied to V_{DD} before it transitions to V_{DD} minimum. The anomaly is *not seen* when the application of power to the RAD_{PAL} starts at zero volts and transitions monotonically to V_{DD} minimum and the slew rate is greater than 0.1V/S.

The anomaly is not wafer lot dependent and affects all date code shipped.

Solution:

The UT22VP10 RAD_{PAL} is susceptible to this POR anomaly whenever residual voltages of between 200mV and 500mV are on the V_{DD} pin(s) prior to the application of the 5V power supply.

In order to avoid powering up the UT22VP10 RAD_{PAL} into a test mode, the following specifications must be met:

- 1) The application of voltages on the V_{DD} pin(s) of the RAD_{PAL} must start at 0V and reach 1V at a rate of 0.1V/s or faster.
- 2) The power-up voltage must be continuously increasing with respect to time, through 3V, and monotonic thereafter.
- 3) No voltage can be applied to V_{DD} prior to the intended power-up sequence.

An alternative or additional method to guarantee that the UT22VP10 RAD_{PAL} functions in the user mode of operation is to implement the following fix into the board level design:

- 1) Apply one of the opcodes shown in Table 1 to the corresponding inputs of the RAD_{PAL}. Notice that the Clock and I9 inputs must have a logic “1” applied during the application of a valid opcode.

Table 1: Valid Power-Up Opcodes

Mode of Operation	Power-Up Opcode (HEX) ¹	RAD _{PAL} Input Pins									
		I 9	I 8	I 7	I 6	I 5	I 4	I 3	I 2	I 1	Clk/I
0	DC	1	1	1	0	1	1	1	0	0	1
2	DE	1	1	1	0	1	1	1	1	0	1
3	DF	1	1	1	0	1	1	1	1	1	1
4	E0	1	1	1	1	0	0	0	0	0	1
5	E1	1	1	1	1	0	0	0	0	1	1
6	E2	1	1	1	1	0	0	0	1	0	1

Notes: 1. The Hexadecimal power-up opcode refers to the RAD_{PAL} inputs I8 - I1.

- 2) Apply one of the opcodes from Table 1 for at least 100ns anytime after V_{DD} is within $5V \pm 10\%$ to ensure all test mode latches are cleared. Figure 1 shows the opcode timing diagram.

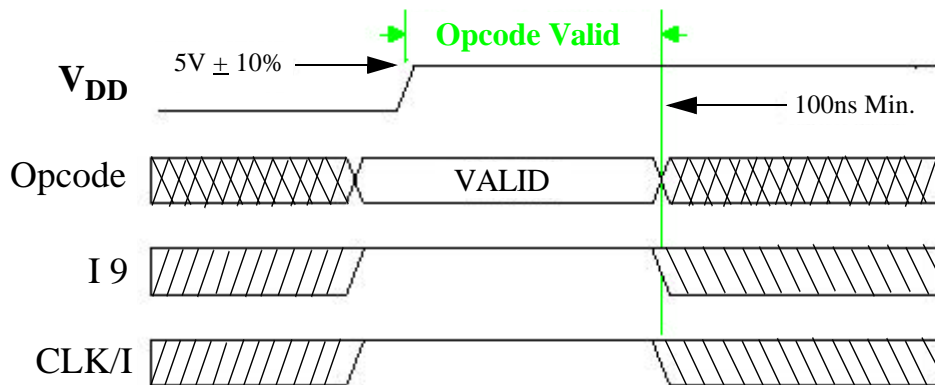


Figure 1. Opcode Timing

Applying one of the opcodes from Table 1 enables the programmed security fuse to reset the internal test latch, forcing the UT22VP10 RAD_{PAL} into the user mode of operation.