

UT699 PCI Reset and Clock Requirements

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC* Number:
UT699 32-bit Fault-Tolerant SPARC V8/LEON 3FT Processor	UT699	5962-08228	01, 02	WG07

* PIC = Product Identification Code

1 Overview

The UT699 Leon 3FT microprocessor system-on-chip includes a PCI core that can be configured for 32-bit, 33MHz operations. The PCI core requires proper initialization even when PCI is not utilized. If proper initialization requirements are not met, the PCI core can lock up the internal AMBA bus in some instances causing the entire processor to lock up. This lockup condition is identified by the processor performing a single access to PROM at address 0x0 following the de-assertion of $\overline{\text{RESET}}$ with no subsequent PROM accesses occurring. This advisory explains the requirements for PCI initialization. The initialization sequence is required during the power-up sequence after which time the PCI core may be utilized normally as described in **Chapter 9.0 PCI Target / Master Unit** of the *UT699 Functional Manual*. Thereafter, each time power is cycled, the system must perform the initialization sequence. Timing requirements for PCI clock gating are also discussed.

2 PCI Initialization Requirements

2.1 PCI Core Utilized in System

Figure 1 shows the required timing relationship between the PCI clock input and the $\overline{\text{RESET}}$ and $\overline{\text{PCIRST}}$ inputs when the PCI core is utilized. It is assumed that the V_{DD} and V_{DDC} power rails are stable and the SYSCLK input has a valid clock as described in **Section 4.1 Power Sequencing and Reset** of the *UT699 Leon 3FT Data Sheet*. Parameters t_{CVPH} and t_{CVRH} are specified in PCI clock cycles and must be met in order to ensure that the PCI state machine is initialized to idle state prior to the execution of code. $\overline{\text{RESET}}$ may be deasserted after 10 valid PCI clock cycles. There is no timing requirement for $\overline{\text{RESET}}$ relative to $\overline{\text{PCIRST}}$. The PCI core may be held in reset by asserting $\overline{\text{PCIRST}}$ until core utilization is required.

If clock gating is used to reduce power, the PCI clock can be disabled after delaying t_{PLCI} following the assertion of the $\overline{\text{PCIRST}}$. Refer to Table 2 for a summary of the timing parameters.

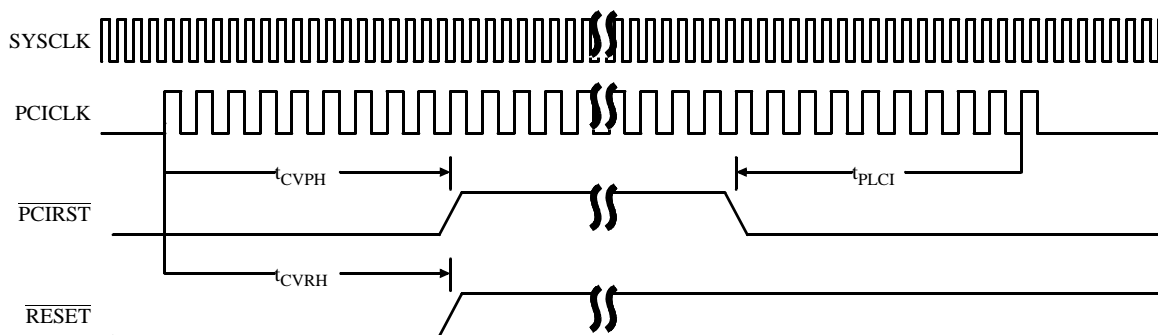


Figure 1. Timing Relationships of Clock and Reset Inputs for PCI Core Utilization

2.2 Initialization of Unused PCI Core

Figure 2 shows the required timing relationship between the PCI clock input and $\overline{\text{RESET}}$ when the PCI core is not utilized. It is assumed that the V_{DD} and V_{DDC} power rails are stable, and that the SYSCLK input has a valid system clock per **Section 4.1 Power Sequencing and Reset** of the *UT699 Leon 3FT Data Sheet*. The critical timing parameter is t_{CVRH} which must be met in order to ensure that the PCI state machine is initialized to idle state. $\overline{\text{RESET}}$ may be deasserted after 10 valid PCI clock cycles. The PCI clock input may be permanently tied low or high immediately following the rising edge of $\overline{\text{RESET}}$. Since PCI is not being used, $\overline{\text{PCIRST}}$ is permanently tied to V_{SS} .

Refer to Table 2 for a summary of critical and recommended timing parameters.

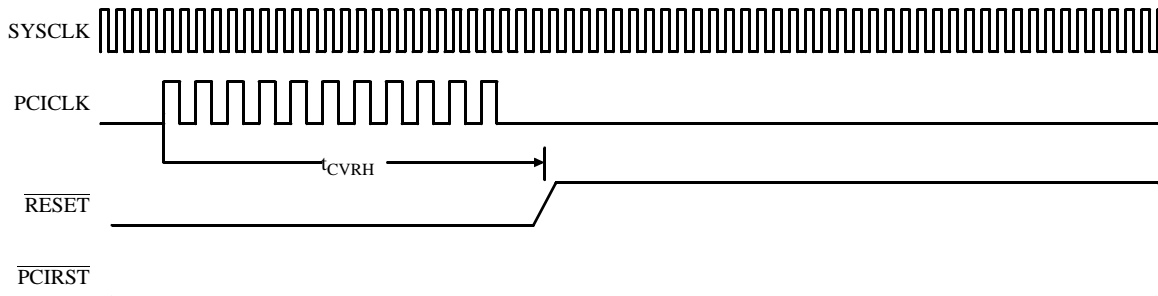


Figure 2. Timing Relationships of Clock and Reset Inputs for Unused PCI Core

2.3 Timing Summary

The following table summarizes the required and recommended timing parameters to ensure proper PCI core and system operation.

Table 2: Summary of Timing Parameters

Symbol	Description	Min	Max	Units
t_{CVRH}	PCICLK \uparrow to $\overline{\text{RESET}}$ deassertion	10	--	PCI clocks
t_{CVPH}	PCICLK \uparrow to $\overline{\text{PCIRST}}$ deassertion	10	--	PCI clocks
t_{PLCI}	$\overline{\text{PCIRST}}$ assertion to PCICLK invalid	10	--	PCI clocks