

UTMC Product Advisory

UT80CRH196KD and UT80C196KD Anomaly List Cross Reference

1.0 Introduction:

This product advisory provides a cross reference of product advisories and errata sheets which provide detailed discussions of the individual anomalies identified in the “A” and “B” revisions (PIC# JD02A and JD02B respectively) of the UT80CRH196KD and the UT80C196KD. The corresponding product advisories and erratas sheets are posted on the UTMC Web site (<http://www.utmc.com>).

2.0 JD02A Anomalies:

The anomalies identified in the JD02A version of the UT80CRH196KD and the UT80C196KD microcontroller are listed below. Furthermore, all anomalies that have been identified in the JD02B version of the UT80CRH196KD and the UT80C196KD are applicable to the JD02A.

1. Writing to the IOS2 SFR will allow the user to set and clear the HSO pins.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

2. \overline{BHE} is only available during writes, it should also be available for reads.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

3. The CCB data is internally latched as zeroes when a wait state is requested during the CCB fetch.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

4. When IOC1.2 is low, the Timer1 overflow status in IOS1.5 is not updated.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

5. The IOS2 event status bits are only set if the HSO command actually changes the state of a pin. Under correct operation, the IOS2 event status bits should be set whenever an HSO command is executed, regardless of the previous state on the HSO pins.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

6. Pending interrupts are processed by a standard interrupt service routine if the PSE bit is inactive, even if the particular interrupt is enabled in the PTS_SEL SFR. Under correct operation, if an interrupt is enabled in the PTS_SEL SFR, then it should automatically be disabled for standard interrupt processing, independent of the state of the global PTS enable (PSE) bit.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

UTMC Product Advisory

7. When a byte shift instruction is executed with a with an odd address operand, the result is stored in the odd address, but the source data is fetched from the even byte of the address.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

8. IOS0 bits 6 and 7 are not write protected.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

9. The assertion of the $\overline{\text{BHE}}$ signal coincides with the assertion of the $\overline{\text{WR}}$ signal. The falling edge of $\overline{\text{BHE}}$ should occur one state time earlier.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

10. The alternate function of port pins P1.5, P1.6, and P1.7 are not disabled when the UT80CRH196KD and UT80C196KD are configured for DMA operation.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

11. The alternate function of port pin P2.6 is not disabled when this port pin is configured as the T2UP_DN control input.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

12. Loading the HSO CAM using the PTS block transfer mode does not guarantee time between writes to allow the Holding Register to empty.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

And is further documented in the product erratas directory identified above under the title:

[UT80CRH196KD PTS Servicing of the HSO Module \(PIC# JDO2A\) June 1998; 11K pdf](#)

13. The undefined PTS modes 2, 5, and 7 should perform single transfers. Instead they perform transfers to unpredictable addresses.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

14. The INST pin on the UT80CRH196KD and UT80C196KD is not active for all instruction fetches that immediately follow an external data memory access.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

UTMC Product Advisory

15. The global PTS enable signal (PSE) located in the Program Status Word (PSW) gets the value of the global interrupt enable (EI) bit of the PSW during a POPF instruction.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

16. The CCB address is placed on the external address/data bus one state time prior to the ALE rising edge.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

17. Reception of the first serial data character following and applications code generated parallel write to the SBUF_RX SFR on the UT80CRH196KD and the UT80C196KD causes the SP_STAT SFR to flag an Overflow Error by setting its OE bit.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

18. The TXE bit of the SP_STAT SFR is not valid when read immediately following a write to the SBUF_TX SFR.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

19. Writing to bits 7:2 of the SP_STAT SFR can set or clear any of these bits. Under correct operation, the application code should only be able to set bits 7:4 and bit 2. The TXE bit (bit 3) should always be write protected.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

20. Using a 2-byte PTS block write into the SBUF_TX SFR (when TXE is high) causes the second byte to be corrupted.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

21. After returning from an interrupt, the instruction queue fills before the microcontroller jumps to a previously pending interrupt which then empties the instruction queue.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

22. The TXD clock signal is not defined on reset. The unknown value can be seen if the SPCON is written to Serial Mode 0 before the baud register is written.

This anomaly is described in the product advisories directory identified above under the title:

[UT80CRH196KD Design Bugs in 1ST Pass Silicon \(PIC# JD02A\) 2/99; 13K pdf](#)

UTMC Product Advisory

3.0 JD02B Anomalies:

The anomalies identified in the JD02B version of the UT80CRH196KD and the UT80C196KD microcontroller are listed below. Furthermore, all anomalies that have been identified in the JD02B version of the UT80CRH196KD and the UT80C196KD are applicable to the JD02A.

1. Interrupts will not occur if HSI Data Loaded is the interrupt source for INT02 and any previous events remain in the HSI FIFO.

This anomaly is described in the product erratas directory under the title:

[UT80CXX196KD MicroController Revision B \(JD02B\) HSI Interrupt and I/O Status Bits Anomalies](#) 8/99

2. The bits in the IOS1 and IOS2 SFRs that are cleared upon a read may not report an event if it occurs at the same time as a read of these register.

This anomaly is described in the product erratas directory under the title:

[UT80CXX196KD MicroController Revision B \(JD02B\) HSI Interrupt and I/O Status Bits Anomalies](#) 8/99

3. Writes into the T2RST_EVENT bit (IOS2.6) are not accepted. The double registering of the T2RST_EVENT causes any software-written bit changes to be over-written by the HSO module.

This anomaly is described in the product erratas directory under the title:

[UT80CXX196KD MicroController Revision B \(JD02B\) HSI Interrupt and I/O Status Bits Anomalies](#) 8/99

4. The ALE signal contains a noise glitch of more than 0.5V whenever the address/data and EDAC busses switch from high to low at the same time.

This anomaly is described in the product application notes directory under the title:

[UT80CXX196KD MicroController \(JD02*\) ALE Considerations](#) 5/99

5. Instruction fetches from slow program memory requiring wait-states cause the microcontroller to lock-up when the source operand is fetched from internal memory with indexed or indirect memory addressing modes.

This anomaly is described in the product erratas directory under the title:

[UT80CXX196KD MicroController \(JD02B\) Controller Wait State Anomaly](#) 8/99

6. Instruction fetches from slow program memory requiring wait-states cause delays in the CMPL instruction, which causes the microcontroller to re-latch incorrect data at every clock edge.

This anomaly is described in the product erratas directory under the title:

[UT80CXX196KD MicroController \(JD02B\) CMPL Operaton with Wait-State](#) 8/99

7. The overflow flag of the PSW (V flag) is not properly cleared by the following instructions: ADDC, CLR, AND, OR, XOR.

This anomaly is described in the product erratas directory under the title:

[UT80CXX196KD MicroController \(JD02B\) ALU Anomaly](#) 8/99

UTMC Product Advisory

4.0 JD02C Anomalies:

The anomalies identified in the JD02C version of the UT80CRH196KD and UT80C196KD microcontroller are listed below. Furthermore, all anomalies that have been identified in the JD02C version of the UT80CRH196KD and the UT80C196KD are applicable in the JD02A and JD02B.

1. The NORML instruction described by the MCS-96 instruction set architecture does not report a 00h value in the destination operand when the source operand is negative.

This anomaly is described in the product erratas directory under the title:

[Will be available 1Q00](#)

2. Using the HSO unit to reset Timer 2 always results in a software timer interrupt (INT05), regardless of whether the T2RST CAM entry disables the interrupt when the command is executed.

This anomaly is described in the product erratas directory under the title:

[Will be available 1Q00](#)

3. The external Timer 2 reset pins are level sensitive. The correct operation of the external Timer 2 reset pins should be sensitive to the rising edge of reset signal.

This anomaly is described in the product erratas directory under the title:

[Will be available 1Q00](#)

The C revision of the UT80CXX196KD includes corrections of all anomalies found in the JD02A and JD02B version of the microcontroller. UTMC will correct the remaining anomalies (found in JD02C) through a D revision of the JD02 mask set. JD02D prototypes will be available late in 2Q00, and production units will be available in 3Q00.