Standard Products

UT8R512K8 512K x 8 SRAM

Data Sheet
March 2009
www.aeroflex.com/memories

FEATURES

- ❑ 15ns maximum access time
- ❑ Asynchronous operation for compatibility with industry-standard 512K x 8 SRAMs
- ❑ CMOS compatible inputs and output levels, three-state bidirectional data bus
  - I/O Voltage 3.3 volts, 1.8 volt core
- ❑ Operational environment:
  - Intrinsic total-dose: 300K rad(Si)
  - SEL Immune >100 MeV-cm^2/mg
  - LET$_{th}$ (0.25): 53.0 MeV-cm^2/mg
  - Memory Cell Saturated Cross Section 1.67E-7cm^2/bit
  - Neutron Fluence: 3.0E14n/cm^2
  - Dose Rate
    - Upset 1.0E9 rad(Si)/sec
    - Latchup >1.0E11 rad(Si)/sec
- ❑ Packaging options:
  - 36-lead ceramic flatpack (3.762 grams)
- ❑ Standard Microcircuit Drawing 5962-03235
  - QML Q & Vcompliant part

INTRODUCTION

The UT8R512K8 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by taking chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the eight I/O pins (DQ0 through DQ7) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (DQ0 through DQ7) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).

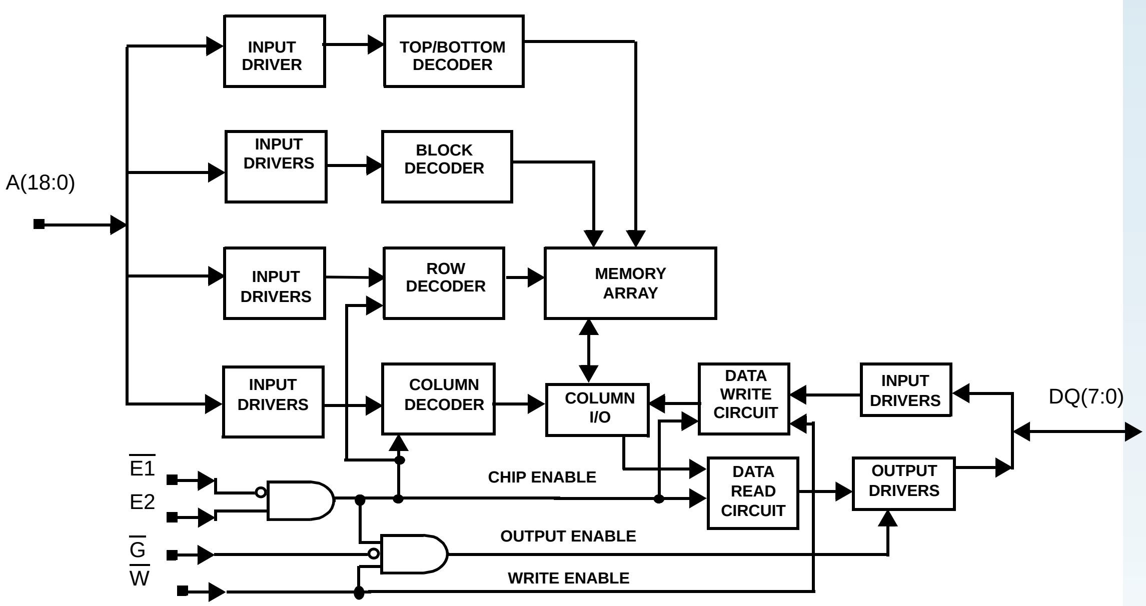


Figure 1. UT8R512K8 SRAM Block Diagram

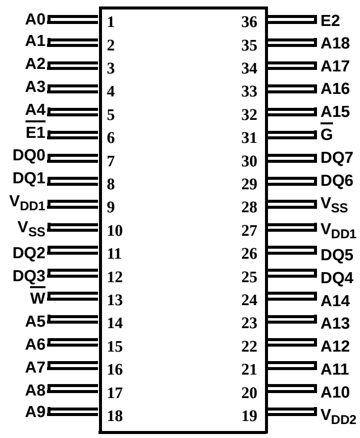


Figure 2. 15ns SRAM Pinout (36)

PIN NAMES

A(18:0)	Address	$\overline{W}$	WriteEnable
DQ(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E1}$	Chip Enable 1 (active low)	V_{DD1}	Power (1.8V)
E2	Chip Enable 2 (active high)	V_{DD2}	Power (3.3V)
		V_{SS}	Ground

DEVICE OPERATION

The UT8R512K8 has four control inputs called Chip Enable 1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). $\overline{E1}$ and E2 device enables control device selection, active, and standby modes. Asserting $\overline{E1}$ and E2 enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	E2	$\overline{E1}$	I/O Mode	Mode
X	X	X	1	3-state	Standby
X	X	0	X	3-state	Standby
X	0	1	0	Data in	Write
1	1	1	0	3-state	Read[2]
0	1	1	0	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}$ and E2 greater than V_{IH} (min) and $\overline{E1}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max) and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the nine bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by either of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by either $\overline{E1}$or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

OPERATIONAL ENVIRONMENT

The UT8R512K8 SRAM incorporates special design and layout features which allows operation in a limited environment.

Table 2. Operational Environment Design Specifications[1]

Total Dose	300K	rad(Si)
Heavy Ion Error Rate[2]	8.9×10^{-10}	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles >100MeV-cm^2/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

Supply Sequencing

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage	-0.3 to 2.1V
V_{DD2}	DC supply voltage	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	5°C/W
I_I	DC input current	±5 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	Positive supply voltage	1.7 to 1.9V[1]
V_{DD2}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	(P) Screening: -25°C (C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

Notes:

1. For increased noise immunity, supply voltage (V_{DD1}) can be increased to 2.0V. If not tested, all applicable DC and AC charateristics are guaranteed by characterization at V_{DD1} (max) = 2.0V.

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IH}	High-level input voltage			$.7*V_{DD2}$		V
V_{IL}	Low-level input voltage				$.3*V_{DD2}$	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, V_{DD2} = V_{DD2} (min)			$.2*V_{DD2}$	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA, V_{DD2} = V_{DD2} (min)		$.8*V_{DD2}$		V
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V			12	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz @ 0V			12	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}		-2	2	μA
I_{OZ}	Three-state output leakage current	V_O = V_{DD2} and $V_{SS,}$ V_{DD2} = V_{DD2} (max) $\overline{G}$ = V_{DD2} (max)		-2	2	μA
I_{OS}[2, 3]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}		-100	+100	mA
$I_{DD1}(OP_1)$	Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD2} = V_{DD2} (max)	V_{DD1} = 1.9V		12	mA
			V_{DD1} = 2.0V		19	mA
$I_{DD1}(OP_2)$	Supply current operating @66MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD2} = V_{DD2} (max)	V_{DD1} = 1.9V		30	mA
			V_{DD1} = 2.0V		43	mA
$I_{DD2}(OP_1)$	Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max) V_{DD2} = V_{DD2} (max)			.2	mA
$I_{DD2}(OP_2)$	Supply current operating @66MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			4	mA

$I_{DD1}(SB)^4$	Supply current standby @ 0Hz	CMOS inputs , $I_{OUT} = 0$ $\overline{E1} = V_{DD2}$ -0.2, E2 = GND $V_{DD2} = V_{DD2}$ (max)	$V_{DD1} = 1.9V$		11	mA
			$V_{DD1} = 2.0V$		18	mA
$I_{DD2}(SB)^4$			$V_{DD1} =$ V_{DD1} (max)		100	µA
$I_{DD1}(SB)^4$	Supply current standby A(18:0) @ 66MHz	CMOS inputs , $I_{OUT} = 0$ $\overline{E1} = V_{DD2}$ - 0.2, E2 = GND, $V_{DD2} = V_{DD2}$ (max)	$V_{DD1} = 1.9V$		11	mA
			$V_{DD1} = 2.0V$		18	mA
$I_{DD2}(SB)^4$			$V_{DD1} =$ V_{DD1} (max)		100	µA

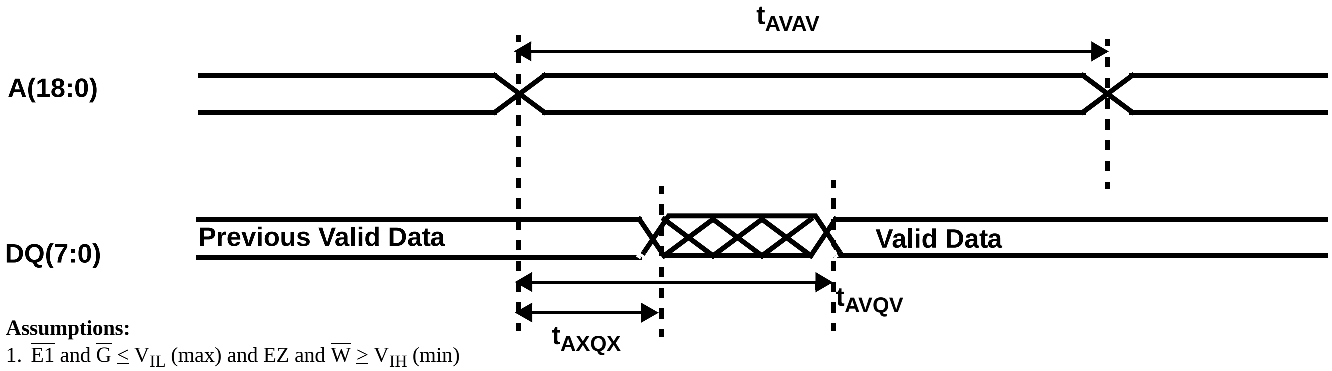
Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. $V_{IH} = V_{DD2}$ (max), $V_{IL} = 0V$.

AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

$V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min); Unless otherwise noted, Tc is per the temperature ordered

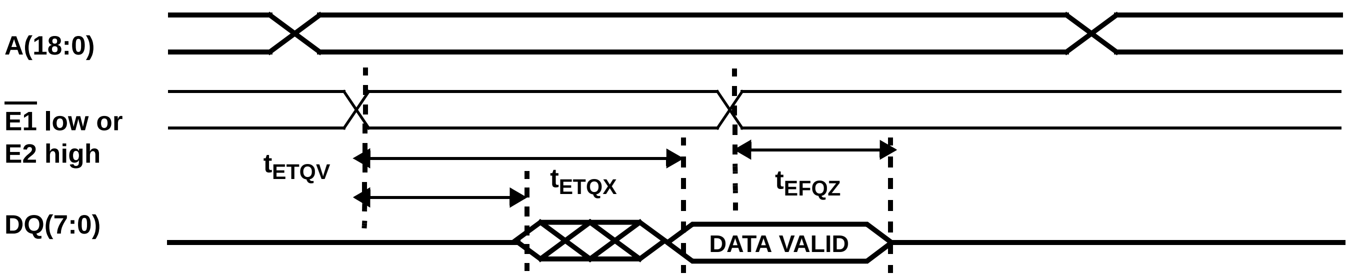
SYMBOL	PARAMETER	8R512-155 MIN	MAX	UNIT
t_{AVAV}[1]	Read cycle time	15		ns
t_{AVQV}	Read access time		15	ns
t_{AXQX}[2]	Output hold time	3		ns
t_{GLQX}[1,2]	$\overline{G}$-controlled output enable time	0		ns
t_{GLQV}	$\overline{G}$-controlled output enable time		7	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		7	ns
t_{ETQX}[2,3]	E-controlled output enable time	5		ns
t_{ETQV}[3]	E-controlled access time		15	ns
t_{EFQZ}[4]	E-controlled output three-state time[2]		7	ns

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Guaranteed, but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (chip enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2. SEU immunity does not affect the read parameters.
4. The EF (chip enable false) notation refers to the latter rising edge of $\overline{E1}$ or falling edge of E2. SEU immunity does not affect the read parameters.



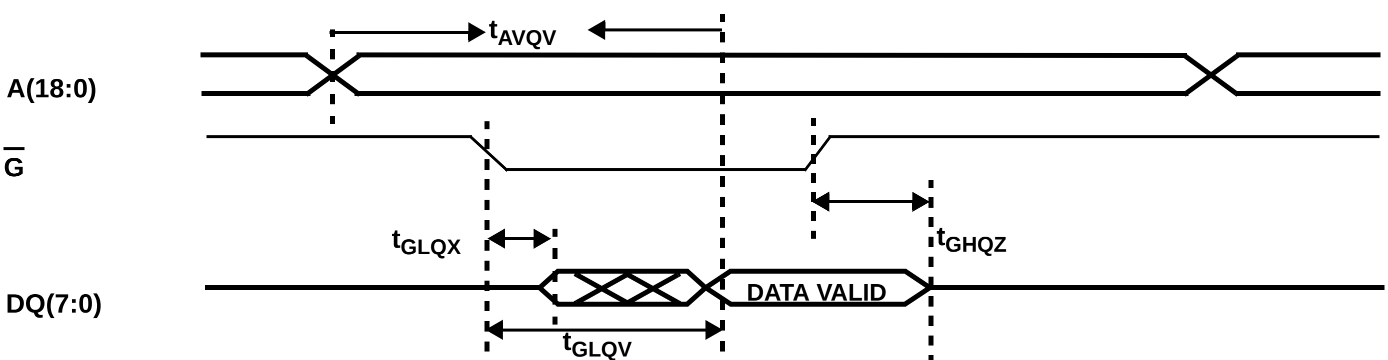
Assumptions:
1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max) and EZ and $\overline{W} \geq V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:
1. $\overline{E1} \leq V_{IL}$ (max) , E2 > and $\overline{W} \geq V_{IH}$ (min)

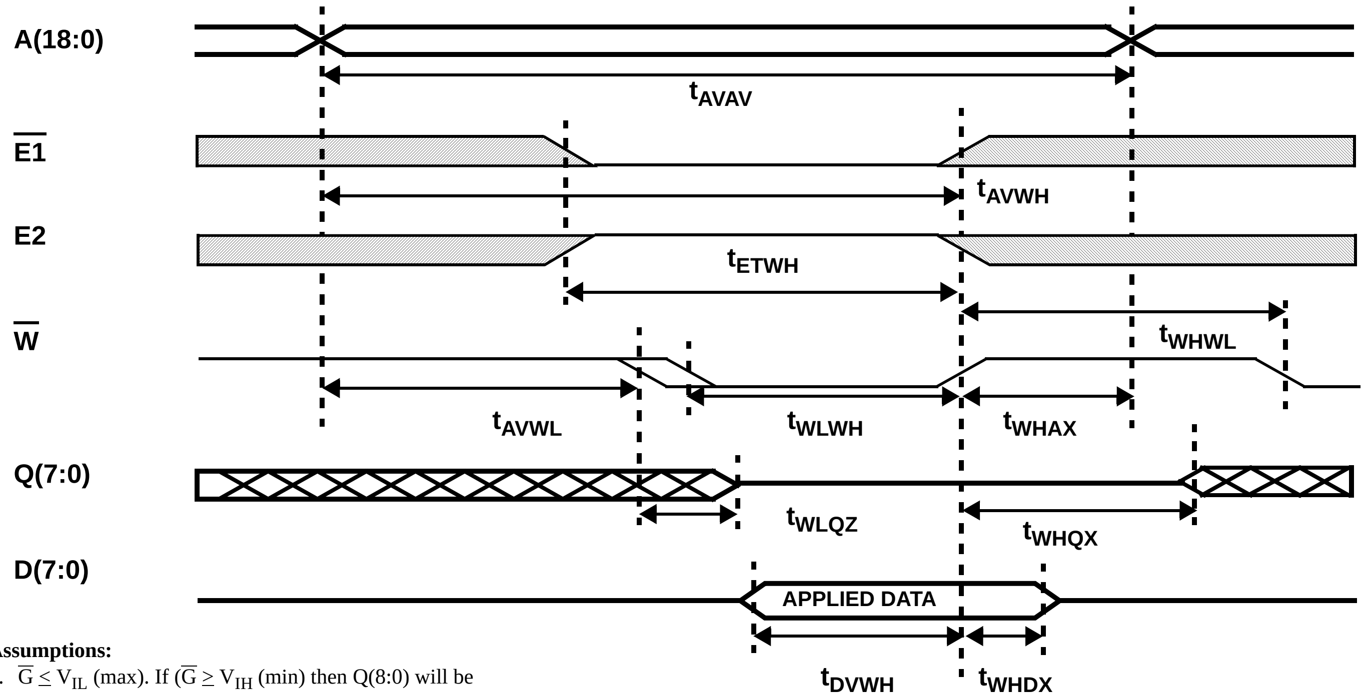
Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

$V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min); Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	8R512-15		UNIT
		MIN	MAX	
t_{AVAV}[1]	Write cycle time	15		ns
t_{ETWH}	Chip enable to end of write	12		ns
t_{AVET}	Address setup time for write ($\overline{E1}$/E2- controlled)	0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	1		ns
t_{WLWH}	Write pulse width	12		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	2		ns
t_{EFAX}	Address hold time for chip enable ($\overline{E1}$/E2- controlled)	0		ns
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		5	ns
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	4		ns
t_{ETEF}	Chip enable pulse width ($\overline{E1}$/E2 - controlled)	12		ns
t_{DVWH}	Data setup time	7		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Chip enable controlled write pulse width	12		ns
t_{DVEF}	Data setup time	7		ns
t_{EFDX}	Data hold time	0		ns
t_{AVWH}	Address valid to end of write	12		ns
t_{WHWL}[1]	Write disable time	3		ns

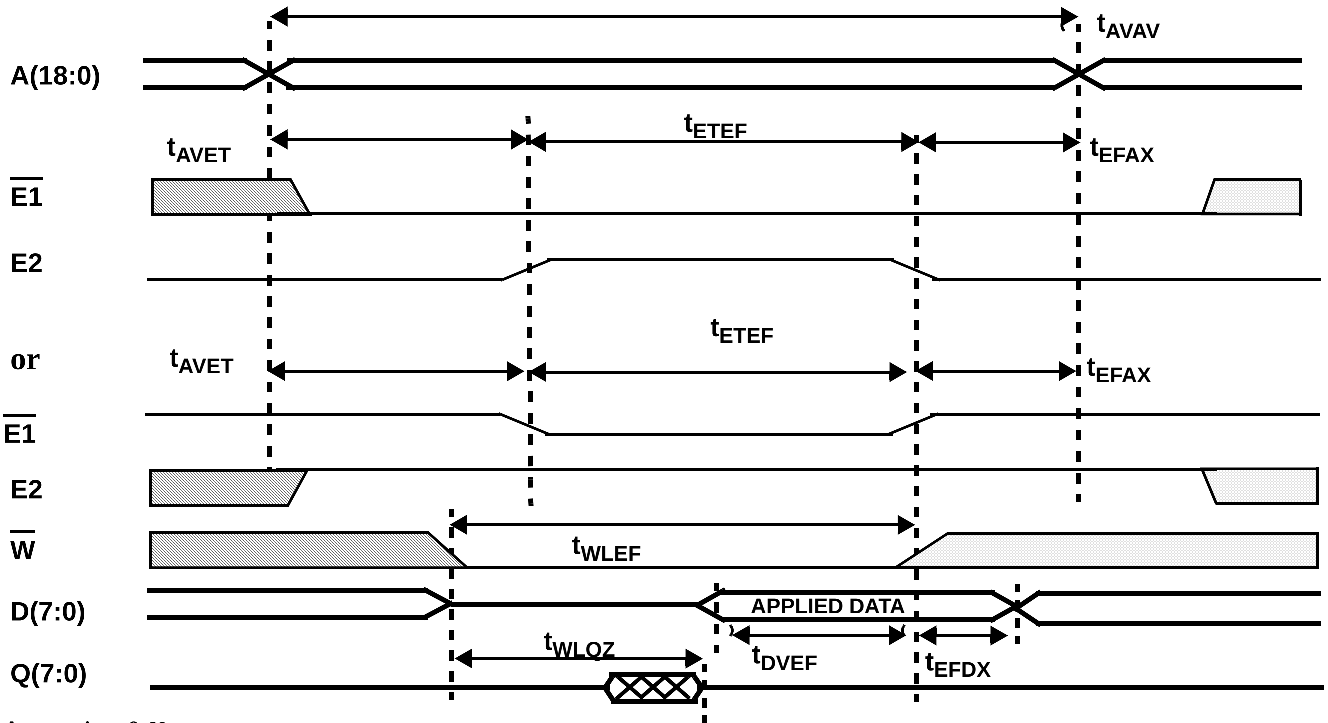
Notes:
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Test with $\overline{G}$ high.
2. Three-state is defined as 200mV change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). If ($\overline{G} \geq V_{IH}$ (min) then Q(8:0) will be in three-state for the entire cycle).

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access



Assumptions & Notes:

1. $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle).
2. Either $\overline{E1}$ scenario above can occur.

Figure 4b. SRAM Write Cycle 2: Chip Enable - Controlled Access

DATA RETENTION CHARACTERISTICS (Pre-Radiation)* (V_{DD2} = V_{DD2} (min), 1 Sec DR Pulse)

SYMBOL	PARAMETER	TEMP	MINIMUM	MAXIMUM	UNIT
V_{DR}	V_{DD1} for data retention	--	1.0	--	V
I_{DDR} [1] Device Type 1	Data retention current	-55°C	--	600	µA
		25°C	--	600	µA
		125°C	--	12	mA
I_{DDR} [1] Device Type 2	Data retention current	-40°C	--	600	µA
		25°C	--	600	µA
		125°C	--	12	mA
t_{EFR} [1,2]	Chip deselect to data retention time	--	0	--	ns
t_R [1,2]	Operation recovery time	--	t_{AVAV}	--	ns

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. E1 = V_{DD2} or E2 = V_{SS} all other inputs = V_{DD2} or V_{SS}
2. V_{DD2} = 0 volts to V_{DD2} (max)

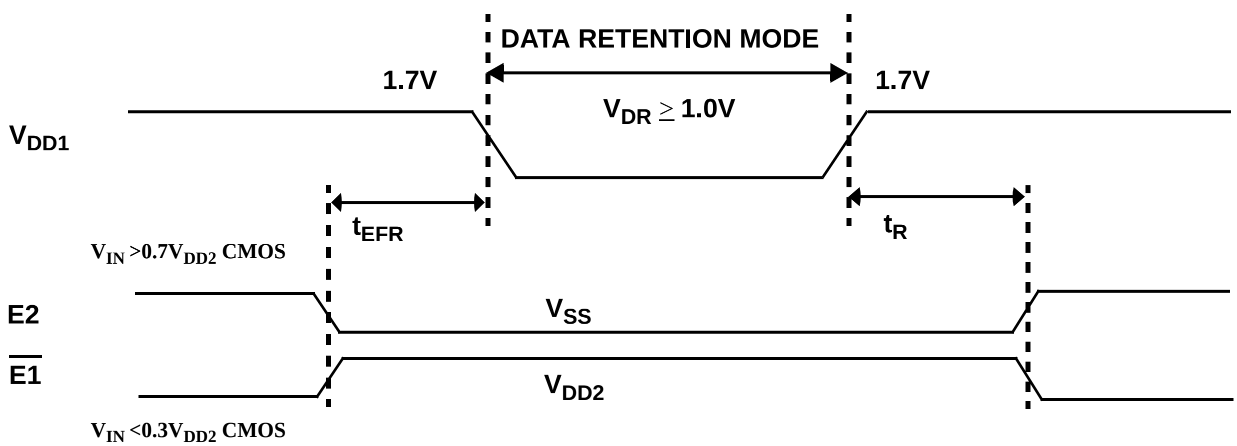
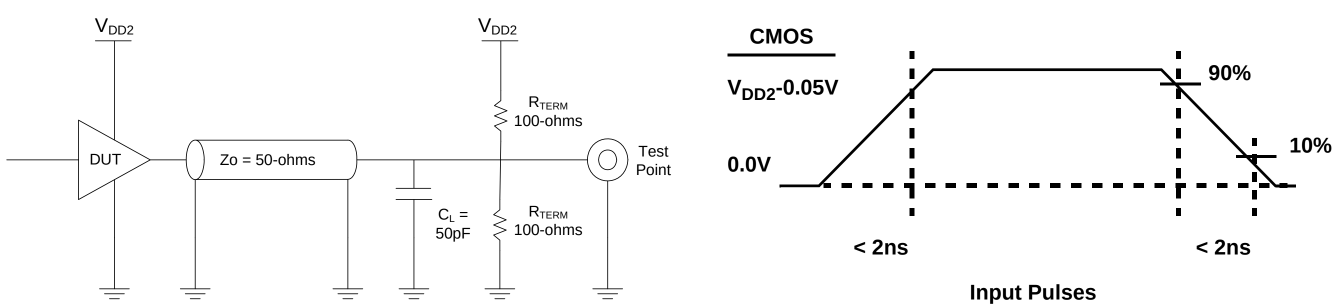
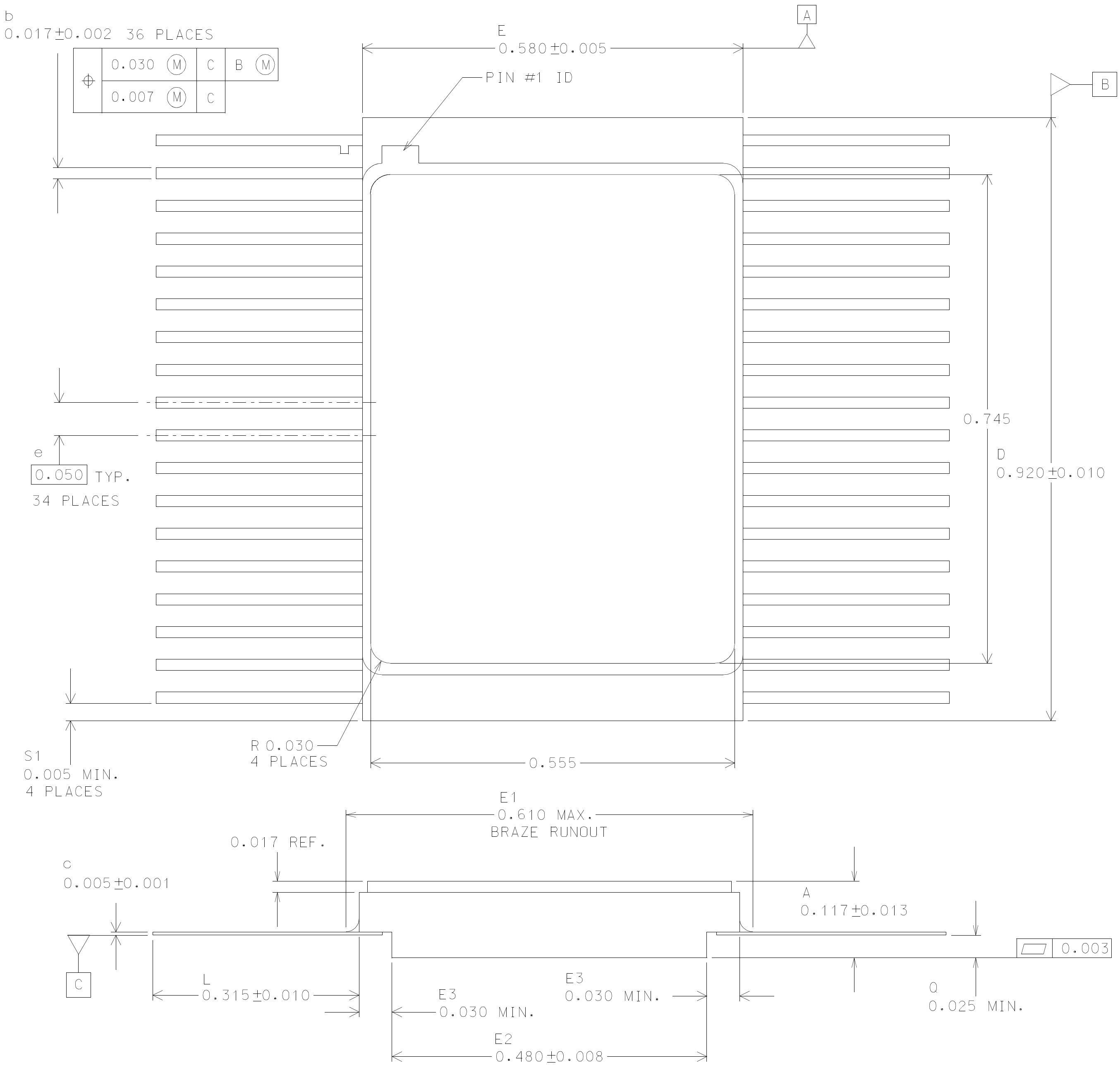


Figure 5. Low V_{DD} Data Retention Waveform



Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$).

Figure 6. AC Test Loads and Input Waveforms

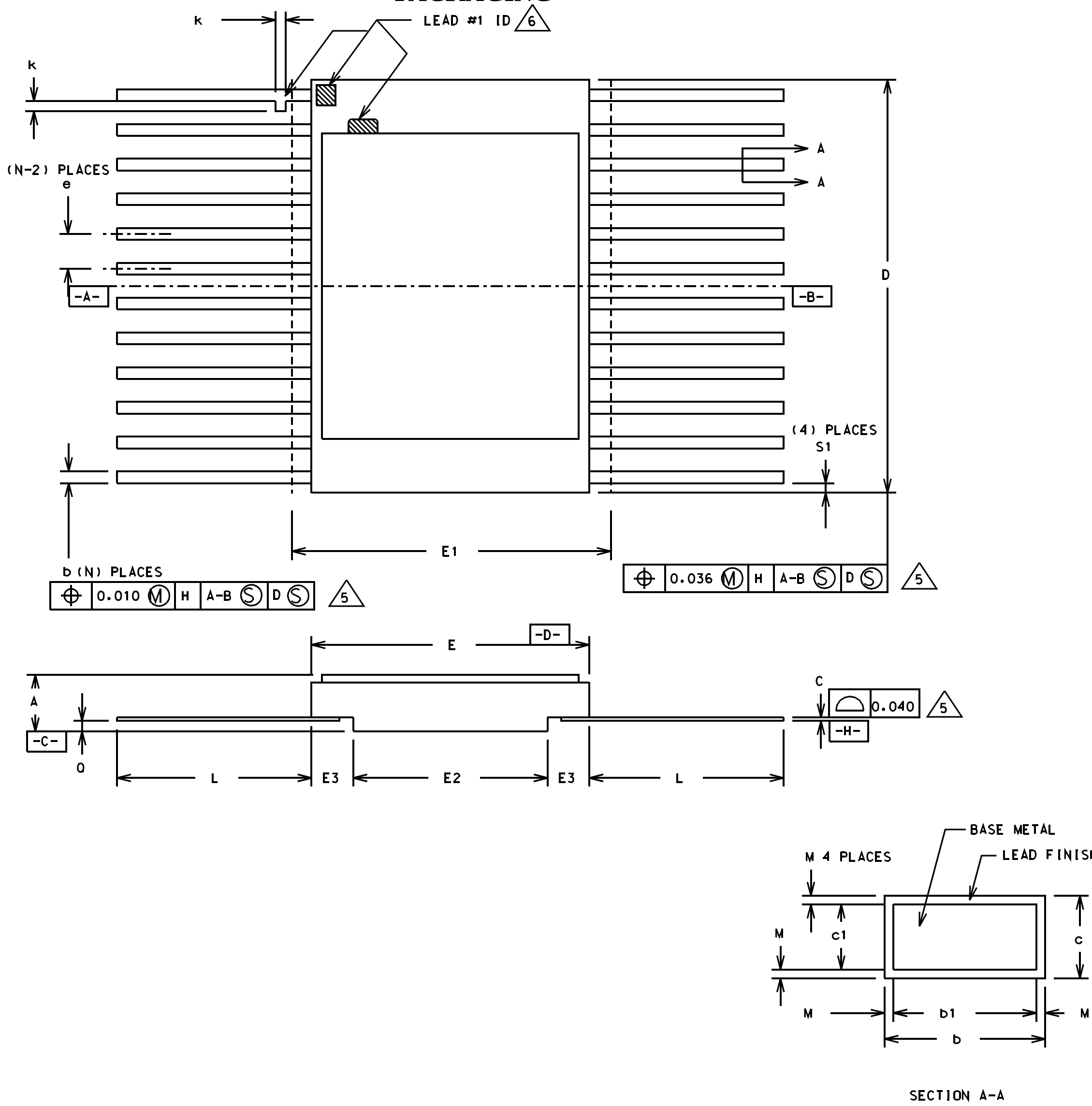


1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Dimension sybology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumerics. One or both ID methods ma y be used for Pin 1 ID.
7. Equivalent to MIL-STD-1853A F-19 configuration A (glass field) using a configuration B (multi-layer) ceramiic body style.

Figure 7. 36-pin Ceramic FLATPACK

LEAD COUNT	DIMENSION SYMBOLS															
	A	b	b1	c	c1	D	E	E1	E2	E3	e	k	L	Q	S1	M
36	0.120 / 0.090	0.020 / 0.015	0.019 / 0.015	0.007 / 0.004	0.006 / 0.004	0.930 / -----	0.588 / 0.572	0.600 / -----	----- / 0.470	----- / 0.040	0.050 BSC	0.015 / 0.008	0.325 / 0.305	0.045 / 0.026	----- / 0.005	0.0015 / ----

PACKAGING



1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Dimension sybology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumerics. One or both ID methods ma y be used for Pin 1 ID.
7. Equivalent to MIL-STD-1853A F-19 configuration A (glass field) using a configuration B (multi-layer) ceramiic body style.

Figure 7. 36-pin Ceramic FLATPACK

ORDERING INFORMATION

512K x 8 SRAM:

UT **** - * * * * *

Lead Finish:
(A) = Hot solder dipped
(C) = Gold
(X) = Factory option (gold or solder)

Screening:
(C) = HiRel Temperature Range flow (-55°C to +125°C)
(P) = Prototype flow
(W) = Extended industrial temperature range flow (-40°C to +125°C)

Package Type:
(U) = 36-lead FP

Access Time:
(15) = 15ns access time

Device Type:
(8R512K8) = 512K x 8 SRAM

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. HiRel Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
5. Extended Industrial Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

512K x 8 SRAM: SMD

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Lead Finish:
(A) = Hot solder dipped
(C) = Gold
(X) = Factory Option (gold or solder)

Case Outline:
(U) = 36-lead ceramic flatpack

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type
(01) = 15ns access time, CMOS I/O, 36-lead flatpack package, dual chip enable (-55°C to +125°C)
(02) = 15ns access time, CMOS I/O, 36-lead flatpack package, dual chip enable (-40°C to +125°C)

Drawing Number: 03235

Total Dose:
(R) = 100K rad(Si)
(F) = 300K rad(Si)

Federal Stock Class Designator: No options

Notes:
1.Lead finish (A,C, or X) must be specified.
2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

NOTES

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

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Tel: 321-951-4164
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A passion for performance.

Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused