

GRSPWROUTER

SpaceWire Routing Switch

Description

The GRSPWROUTER IP core is a VHDL model of a SpaceWire routing switch as defined in ECSS-E-ST-50-12C. The core is highly configurable, flexible and portable to a wide variety of FPGA and ASIC technologies. The core supports all mandatory and optional features in the ECSS-E-ST-50-12C standard and can be configured from the minimum number of 2 ports to the maximum 31, with an additional mandatory configuration port. The configuration port provides access to configuration and status registers and the routing table using the Remote Memory Access Protocol (RMAP) defined in ECSS-E-ST-50-52C. The SpaceWire Plug-and-Play (PnP) protocol can optionally be supported on the configuration port.

Routing

The core uses a non-blocking switch matrix which can connect any input port to any output port. All the addressing modes such as path, logical and regional logical are supported. Group adaptive routing is fully supported, both path and logical addresses can be individually configured to use anyone from 1 up to all ports. A unique feature for the core is the support for packet distribution, each path or logical address can be individually configured to transmit on 1 up to all ports. This can be used to implement multicast and broadcast addresses. Output ports are arbitrated using two priority levels with a round-robin scheme within each level.

Ports

The router ports (except the configuration port) can be individually configured as different types: SpaceWire, FIFO or AMBA ports. They interface to the switch matrix in the same manner but with different external interfaces.

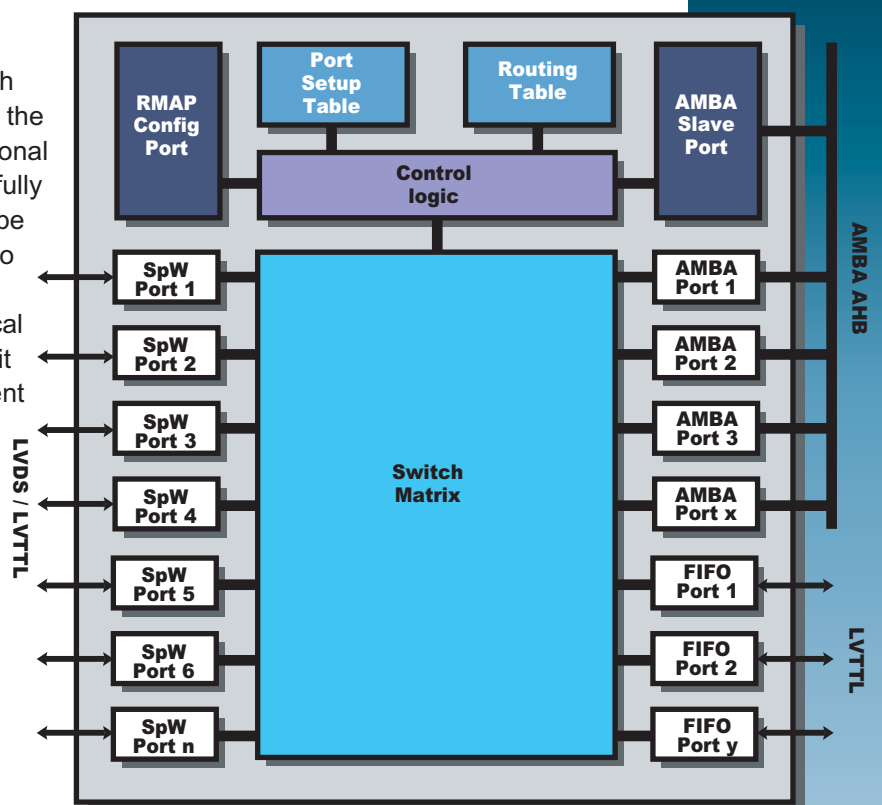
The SpaceWire ports provide standard SpaceWire links using the same codec as in the GRSPW2 core. The router makes use of the codec's unique features such as the configurable receive input and transmit output schemes. The standard self-clocking (XOR) input can be used, or alternatively SDR or DDR sampling. The output can use SDR or DDR. The links can also interface to external Aeroflex UT200SpWPHY01 transceivers. The variety of interfaces makes it possible to reach the highest possible link speed on a wide range of technologies.

The FIFO ports use a 9-bit wide data path in each direction with standard FIFO control signals. This is suitable for providing inter-chip interfaces running on slower clocks.

The AMBA ports provide an interface to an AMBA AHB bus through DMA with an optional RMAP target. The AMBA ports are based on the proven GRSPW2 core with which they are software compatible. This means that existing software drivers can be used when interfacing the router to AMBA based LEON3 and LEON4 processor systems. The AMBA ports can also be used to interface the router to buses such as Mil-Std-1553B, CAN, Ethernet or USB using the cores available in the Aeroflex Gaisler GRLIB IP library.

System-time distribution

Time distribution is supported for all the different port types. Time-code propagation can be individually disabled per port and globally disabled with an external signal. Control flag filtering can optionally be enabled.



Benefits

The different port types along with the high degree of configurability and technology support makes the core suitable for a wide range of systems and allows designers to optimize area and performance. It can be implemented as a standalone router ASIC, FPGA or as part of an AMBA bus based processor system. In each case the router core and its configuration space will be the same, enabling migration to new systems. The core provides numerous interfacing possibilities.

A wide range of configuration registers and signals are provided, giving the user full control of the router, e.g. to disable configuration accesses from certain ports or to filter time-code propagation.

Area and performance

	Actel RTPProAsic3	Actel RTAX	Xilinx Virtex 4
SpW ports	10	10	20
AMBA ports	0	0	11
FIFO ports	2	2	0
Area	40700 VersaTiles / 50 RAM512x18	21500 C / 10200 R / 26 RAM64K36	78000 LUTs / 75 RAM
Core clock	30 MHz	25 MHz	50 MHz
Link rate	180 Mbit/s	200 Mbit/s	200 Mbit/s

Features

- Compliant with ECSS-E-ST-50-12C
- Routing
 - Non-blocking switch-matrix connecting any input port to any output port
 - Path, Logical and Regional Logical addressing
 - Group Adaptive Routing (GAR): from 1 port to all ports for path and logical addresses
 - Packet distribution: from 1 port to all ports for path and logical addresses
 - Two priority levels for output port arbitration
- Configuration port using the RMAP protocol (ECSS-E-ST-50-52C) with optional support for the Space Wire PnP protocol (currently SpaceWire-PnP Protocol Definition, Draft A Issue 2.1)
- Scalable sizing with 2 to 31 ports, each individually configurable as SpaceWire, FIFO or AMBA ports
- SpaceWire ports
 - Up to 31 in a single router
 - Supports high data rates. Up to 200 Mbit/s in both directions on a single link on Actel RTAX and up to 400 Mbit/s on Xilinx Virtex 4
 - Receiver can use self-clocking (XOR), SDR or DDR input sampling
 - Transmitter can use SDR or DDR output
 - Support for external Aeroflex UT200SpWPHY01 SpaceWire Physical Layer Transceiver
 - Support for on-chip and off-chip LVDS transceivers

- AMBA ports
 - Up to 16 in a single router
 - DMA based AHB interface
 - APB interface for control and status
 - Software compatible with the GRSPW2 core
- FIFO ports
 - Up to 31 in a single router
 - 9-bit wide data paths
 - Read/write, full/almost full and programmable empty/almost empty signals
- Core frequency can be down to 1/8 of link rate with support for the maximum throughput
- System-time distribution
 - Supported from all the port types
 - Can be enabled/disabled per port
 - Optional checking of control flags
- Optional AMBA AHB slave interface for access to the configuration space and routing table
- Technology independent design suitable for a wide range of ASIC and FPGA technologies
- Expandable via the AMBA bus to other bus types such as Mil-Std-1553B, CAN, Ethernet and USB
- Optional timers on ports to prevent deadlock

Deliverables

- FPGA/ASIC netlist
- Source code
- Stand-alone testbench
- User's manual
- VxWorks, RTEMS and Linux 2.6 software drivers for the AMBA ports
- Test software

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