

# Semicustom Products

# FPGA to ASIC Conversions

## Fact Sheet

July 2010



### OVERVIEW

Aeroflex Colorado Springs has over 20 years experience in converting FPGA and 3rd-party ASIC netlists into Aeroflex RadHard and non-RadHard ASICs. We maintain a growing database of FPGA and 3rd-party ASIC cell libraries used for conversion, and new cells/macros are added as needed with translations.

Examples of past FPGA conversions and capabilities include:

- Actel: RH1020, RH1280, RT54SX32S/72S, RTAX250S/1000S/2000S
- Xilinx: XC2/3/4000, XC8100, Virtex II Pro/-4/-5
- Altera: EMP5/7000
- Honeywell: HR2/3000, HX2000
- LSI: 5K, 10K, 20K

### ADVANTAGES

- Turnkey FPGA design services -- start to finish
  - FPGA or HDL netlist in > QML certified ASIC out
  - ASIC voltage supply options -- 2.5V or 3.3V core and 3.3V or 5V I/O
  - Form/fit/functional equivalent packages with chip-capacitor attached option
- Automatic test program generation - Aeroflex generates all parametric test patterns
  - NAND Tree ( $V_{IL}/V_{IH}$ ,  $I_{IL}/I_{IH}$ ), Embedded Serial Scan and ATPG
- Dynamic burn-in with high toggle coverage
  - Demonstrated process technology FIT rates < 1
- Formal verification throughout design cycle
  - Original FPGA or HDL netlist remains "golden" reference
  - Formally verified after Scan, JTAG insertion, and after place and route
- Design Flow Requirements
  - Netlist
  - Customer provides STA constraints or functional patterns
  - Aeroflex inserts scan and JTAG, then generates all necessary test program pattern files
- Aeroflex ASIC libraries and processes are well defined and mature (0.6 $\mu$ m, 0.25 $\mu$ m)
- ASIC technology has guaranteed radiation hardness (TID >100K, SEL immune, SEU <1E<sup>-10</sup>)
- Long term foundry agreements in place with high wafer volume production capacity

### PACKAGING

- FPGA-compliant 84, 172, 208, 256 CQFP, 624 CCGA
  - External chip capacitor attachment option available to space quality levels (for improved SSO response)
- All power and ground pins match industry use
- Many other package options available

### DESIGN SYSTEM TOOLKIT

- HDL toolkit supports Verilog HDL and VHDL for synthesis and simulation
- Logic Rules Checker included to verify design connectivity rules are met
- Tester Rules Checker is crucial to verify simulation vectors meet tester constraints
- Schematic capture is still supported, primarily for third-party netlist translations
- Toolkit downloadable from the internet with a password
- Embedded serial scan for high fault coverage

## FPGA vs Industry Comparison (example)

	Actel RH1020/1280	Actel RT54SX32S/72S	UT0.6µm	UT0.25µm
Usable Gates	2K/8K	32K/72K	500K	3M
Feature Size	0.8µm	0.25µm	0.6µm	0.25µm
ASIC Technology	FPGA	FPGA	Gate Array	Standard Cell
Core Voltage	5V	2.5V	3.3V or 5V	2.5V
I/O Voltage	5V	3.3V or 5V	3.3V and/or 5V	3.3V
Cold Sparring/5V Tolerant I/Os	No	Yes	Yes	Yes
PCI/ I/O	No	Yes	No	LVTTL, PCI I/O, PCI Core (Synopsys)
LVDS/PLL	No	No	No	Yes
Max Frequency	60MHz	230MHz	70MHz/215MHz	1.3GHz
Embedded Serial Scan FG>95%	No	No	Yes	Yes
Package - Max # Signal I/O	84/172 CQFP	208CQFP - 173/170 256CQFP - 227/212	84/172 CQFP 208CQFP - 178 256CQFP - 232 Up to 380 I/O	208CQFP - 178 256CQFP - 232 624CCGA - 420 Up to 512 I/O
Chip capacitors on package	No	No	Yes	Yes
TID	1M	100Krad(Si)	300 krad(Si)	>1Mrad(Si)
SEU@125°C	<1E <sup>-8</sup>	<1E <sup>-10</sup>	<1E <sup>-10</sup>	<1E <sup>-12</sup>
SEL	>80MeV	>40MeV	>128MeV Guranteed	>108MeV Guaranteed
Demonstrated reli- ability (FIT rate)	?	?	<1	<1
QML Qualification - Class Q and V	?	?	1998	July 2004

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