Standard Products

Enhanced Bit Rate MIL-STD-1553B Remote Terminal IP

Advanced Datasheet
August, 2008

FEATURES

- VHDL Intellectual Property Source Code
- MIL-STD-1553B Notice II (SAE-AS15531) Compliant
- SAE-AS5652 Enhanced Bit Rate EBR-1553
  - Dual Redundant Remote Terminal (RT)
  - Programmable Baud Rate from 1Mbps to 10Mbps
- Full Transmit and Receive Subbaddress & Mode Code recognition with illegalization control
- Large Receive Subaddress FIFO (512x16)
- Dedicated Transmit Subaddress FIFOs (64x16)
- Separate Transmit FIFO Message Information Word and Time-Tag FIFO (128x16)
- Interrupt Source Register
  - Single Master Interrupt Output
  - Specific Interrupt Source Identification by Bit Fields in the Interrupt Source Register

INTRODUCTION

MIL-STD-1553 has long been the standard in HiRel distributed serial communication for aerospace and defense applications. This standard has been updated and is now controlled by the SAE as AS15531 and defines the Electrical, Mechanical, and Functional characteristics of the Data Bus. The 1Mbps standard has been expanded via AS5652 to increase bandwidth to 10Mbps using RS-485 as a physical interface to a star topology.

This ASIC Megacell provides the Remote Terminal operation for Enhanced Bit Rate (AS5652) and MIL-STD-1553B NII (AS15531) applications. The EBR1553B IP is optimized for embedded SRAM architectures. The design employs a flexible host interface supporting 8- or 16-bit data busses and mail box-like message storage in extensive FIFO memory blocks. Direct memory read/write cycles are used to access the configuration, status, and mode code registers.

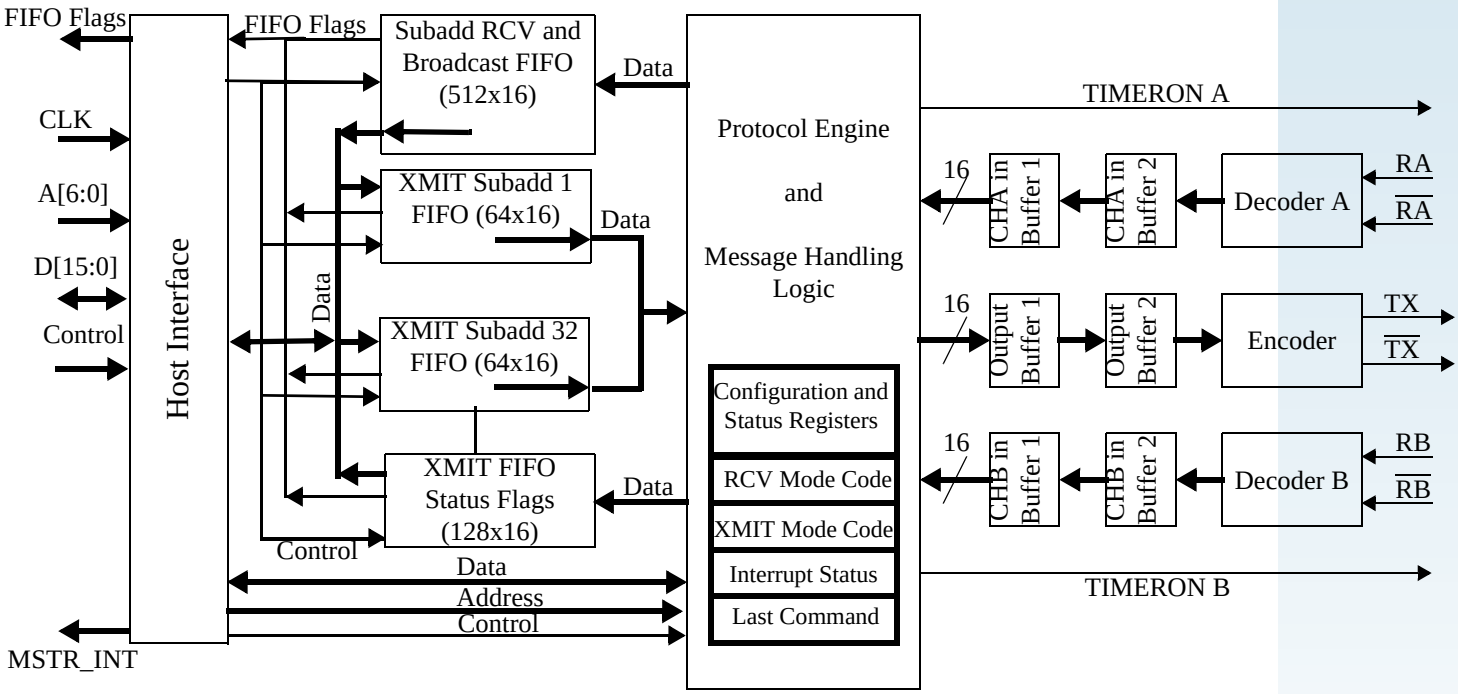


Figure 1: Functional Block Diagram

Overview IP Core

Aeroflex's Remote Terminal IP core is intended to be a complete solution for a dual redundant MIL-STD-1553B, Notice 2 remote terminal (1 MBPS) and is also compatible with SAE AS5652 (10 MBPS**).** The following information gives guidelines on using the Aeroflex 1553 Remote Terminal IP.

The interface to this core is based around individual FIFO mailboxes that store terminal data for each transmit subaddress and a single, shared, FIFO for receive and broadcast message data.

There are two decoders monitoring each of the redundant buses and one encoder that can respond on either bus. The RT Logic interprets the received commands and responds appropriately.

Design Environment
Aeroflex's Remote Terminal IP core is written in VHDL as are all test benches. The IP was simulated using ModelSim 6.0, but is compatible with other simulators. The IP is synthesized using Leonardo Spectrum, but is synthesizable with most tools.

I/O Signal Description

Signal Name	I/O	Description
sysclk	In	System Clock Input- minimum frequency for 1 Mbps operation is 6MHz; minimum frequency for 10 Mbps operation is 60MHz
async_reset	In	Asynchronous Reset
rt_addr (4 : 0)	In	Remote Terminal Address
rt_addrp	In	Remote Terminal Address Parity (Odd parity)
ext_read	In	External Read Advance
ext_write	In	External Write Enable
ext_address (5 : 0)	In	External Address
ext_data_in (15 : 0)	In	External Data Input
rxa	In	Positive decoder input for bus A
rxa_c	In	Negative decoder input for bus A
rxb	In	Positive decoder input for bus B
rxb_c	In	Negative decoder input for bus B
ext_data_out(15 : 0)	Out	External Data Output
enc_done_out	Out	Encoder is done processing a word
dec_ready	Out	Decoder is ready with new data
full_out	Out	Full Status flag for Addressed FIFO, otherwise shows RX FIFO Full Status
empty_out	Out	Empty status flag for addressed FIFO, otherwise shows RX FIFO Empty Status
half_full_out	Out	Half-Full Status flag for Addressed FIFO, otherwise shows RX FIFO Half-Full Status
txinhibit_a	Out	Tells transceiver for bus A to inhibit transmission
txinhibit_b	Out	Tells transceiver for bus B to inhibit transmission
txa	Out	Positive encoder output for bus A
txa_c	Out	Negative encoder output for bus A
txb	Out	Positive encoder output for bus B
txb_c	Out	Negative encoder output for bus B

error_flag	Out	Indicates the last message had an error condition
busy_1553	Out	Status flag to indicate the terminal is busy
done_1553	Out	Status flag to indicate the terminal is done processing a message
msg_rcv_1553	Out	Status flag to indicate that the terminal has received a message

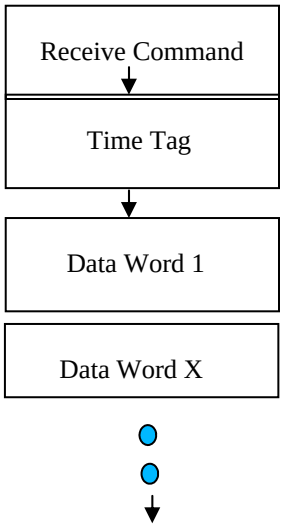
Mode Codes:
Not all mode codes are used in this design. If the mode code is not defined, it will behave as though it is an illegal mode code and respond with the message error bit set in the status word.

Mode Code	T/R Bit	Function
10001	0	Synchronize (with data word)
00001	1	Synchronize (without data word)
00010	1	Transmit Status Word
00100	1	Transmitter Shutdown
00101	1	Override Transmitter Shutdown
00110	1	Inhibit Terminal Flag Bit
00111	1	Override Inhibit Terminal Flag Bit
01000	1	Reset Remote Terminal
10000	1	Transmit Vector Word
10010	1	Transmit Last Command Word

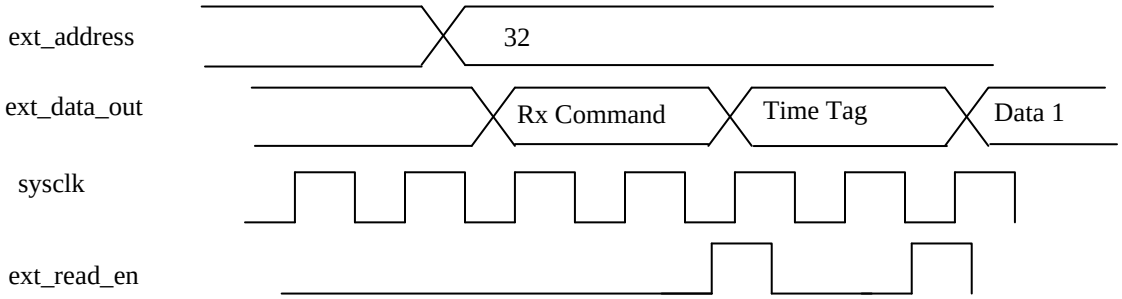
Illegalization:
Mode code Illegalization can be achieved through writing to the mode code illegalization registers. Changing the state of an undefined mode code will not change the response. The terminal will still see the mode code as invalid.
Registers 45, 46 are used to illegalize receive mode codes
Registers 47, 48 are used to illegalize transmit mode codes
Registers 55, 56 are used to illegalize broadcast mode codes for transmit and receive

Subaddress Illegalization – There are three sets of illegalization registers that relate to each subaddress. The user can illegalize each subaddress for receive commands, transmit commands or broadcast commands.
Registers 49, 50 are used to illegalize receive messages to a subaddress
Registers 51, 52 are used to illegalize transmit messages to a subaddress
Registers 53, 54 are used to illegalize broadcast messages to a subaddress

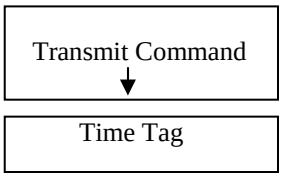
FIFO Interface:
Receive FIFO : The receive FIFO is 511 words deep. Each non-mode code receive command is stored in this FIFO. The message stored in the FIFO is the receive command followed by the Time Tag followed by the number of received words. Each message will occupy between 3 and 34 words. Only valid receive messages will be written to this FIFO.



Reading from the FIFO is a post advance type of read where the data is read then the address is advanced.

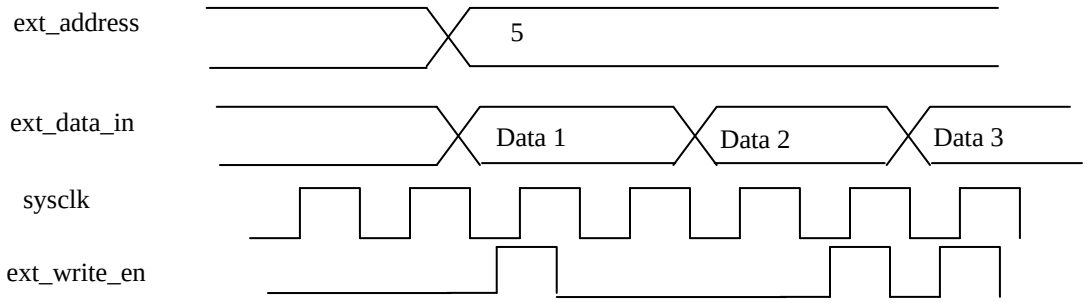


Transmit Message Information FIFO: This FIFO contains the transmit commands that the terminal has received along with a Time Tag for the command. This FIFO is 128 words long and each message will occupy 2 words. Only valid transmit commands will be written to this FIFO.



Transmit Data FIFO's 1-30: These FIFO's contain the data to be transmitted by the terminal when it receives a valid transmit command. The FIFO number corresponds to a particular subaddress. For example a transmit command pertaining to subaddress 8 will read from FIFO 8 and transmit that data out. Each FIFO is 64 words long to enable buffering a maximum of two full-size 1553 transmit subaddress messages.

Writing to the transmit FIFOs is achieved by setting up the data and address and asserting ext_write_en. The data is written into the FIFO on the positive clock edge when ext_write is high.



Status Word Bits:
There are four status bits that the user can customize. One of these bits will be set by the remote terminal when a FIFO underrun or overrun condition occurs. This defaults as the busy bit, but can be changed to the terminal bit based on a pre-synthesis parameter in the bcrtm_defs.vhd file called busy_term_b. This condition will be OR'd with the state of the status_bits register. The other bits directly reflect the condition of this register.

--Status Bits(3) = Service Request
--Status Bits(2) = Busy
--Status Bits(1) = Subsystem
--Status Bits(0) = Terminal

Pre-synthesis parameters:
Aeroflex's IP core needs to know certain things about the operating environment to function properly. There are several parameters that need to be set in the bcrtm_defs.vhd, decoder_defs.vhd, and encoder_defs.vhd files. These parameters vary based on the desired operating speed (10MBPS/1MBPS), as well as the clock speed.

bcrtm_defs.vhd:

rtrt_no_response: Number of clocks to wait before being considered a no-response for RT-RT transfer

no_response_count: No response count for normal commands

legal_gap_count: Number of additional clocks to wait in order to make desired response time.

res_count: Number of clocks to determine resolution of Time Tag Counter

busy_term_b: Selects whether to set busy or terminal due to empty or full condition.

decoder_defs.vhd:

half_bit_count: Sampling counter. Must equal half_bit_time/system clock period minus 1

contig_count: counter used to determine if data is contiguous

encoder_defs.vhd:

half_bit_count: Count value used to determine when to output the next half bit

wait_count: Wait state count to activate transceiver before sending data

fail_count: Fail safe timeout counter to shutdown transceivers

Address Map:
There are six address bits to allow 64 unique addresses.

Address	Name	Description
0	N/A	Not Currently Used
1-30	Transmit Data FIFOs	Allows writing to the Transmit FIFO's as shows the addressed FIFO's status flags.
31	N/A	Not Currently Used
32	Receive Message FIFO	Allows reading from the Receive FIFO
33	Transmit Message Information FIFOs	Allows reading of Transmit Command FIFO, displays status
34	Transmit FIFO Full Flags Status	Outputs full status for transmit FIFO's 15 to 1 respectively on data bus bits [15-1] respectively. Data 0 is low because it is a don't care
35	Transmit FIFO and Receive FIFO, Full Flags Status	Outputs full status for Receive FIFO on data 15 and Transmit FIFO's 30 – 16 on data [14:0]
36	Transmit FIFO, Half_Full Flags Status	Outputs half_full status for FIFO's 15 – 1 on data bus 15 – 1 data 0 is low
37	Receive and Transmit Half_Full Flags Status	Outputs half_full status for Receive FIFO on data 15 and Transmit FIFO's 30 – 16 on data 14 - 0
38	Transmit FIFO Empty Flag Status	Outputs empty status for FIFO's 15 – 1 on data bus 15 – 1, data 0 is low
39	Receive and Transmit FIFO Empty Flag Status	Outputs empty status for Receive FIFO on data 15 and Transmit FIFO's 30 – 16 on data 14 – 0
40	Status Word Bits	Allows write to writable status bits from data 3 - 0 --Status Bits(3) = Service Request --Status Bits(2) = Busy --Status Bits(1) = Subsystem --Status Bits(0) = Terminal
41	N/A	Not currently used
42	Vector Word	Allows write to vector word
43	Read Error Register	Read Error Register
44	Timer Tag	Read/Write to time tag register
45	Receive Mode Code Illegalization Register	Write to illegalize receive mode code register 15:0
46	Receive Mode Code Illegalization Register	Write to illegalize receive mode code register 31:16
47	Transmit Mode Code Illegalization Register	Write to illegalize transmit mode code register 15:0
48	Transmit Mode Code Illegalization Register	Write to illegalize transmit mode code register 31:16
49	Receive Subaddress Illegalization Register	Write to illegalize receive sub-address register 15:0
50	Receive Subaddress Illegalization Register	Write to illegalize receive sub-address register 31:16
51	Transmit Subaddress Illegalization Register	Write to illegalize transmit sub-address register 15:0
52	Transmit Subaddress Illegalization Register	Write to illegalize transmit sub-address register 31:16
53	Broadcast Mode Code Illegalization Register	Write to illegalize broadcast for sub-address register 15:0
54	Broadcast Mode Code Illegalization	Write to illegalize broadcast for sub-

	Register	address register 31:16
55	Broadcast Mode Code Illegalization Register	Write to illegalize broadcast for mode code register 15:0
56	Broadcast Mode Code Illegalization Register	Write to illegalize broadcast for mode code register 31:16
57-63	N/A	Not currently used

Guidelines:

To aid in your design, the following guidelines are included.

1. RT-RT timeout has 54-60us range from the end of the 1st command. The timeout counter does not start counting until the end of the 2nd command. This means that the timeout count depends on the timing between the 1st and 2nd commands. Assume the count happens contiguously; it should be reduced if the 2nd command is delayed.

2. Bus Switching that interrupts a message could cause an error. Due to the FIFO functionality, the message that was interrupted may have already sent data that was pulled out of the FIFO's. There may still be other data that was associated with the same message still in the FIFO.

3. Bus switching during last word of transmit command makes the transmitter believe it sent out all words and will write command to transmit out FIFO.

4. Transmit and Receive Subaddress Illegalization is set up so that the RT does not respond to the command sent to the illegal subaddress.