

July 18, 2007

Dear Customer:

Aeroflex Colorado Springs (Aeroflex) appreciates your interest and use of our products, specifically the UT6325 RadHard Eclipse FPGA. The purpose of this letter is to inform you that the QL9600 programming driver for the UT6325 on the System General T9600 programmer has been revised to improve post-programmed ViaLink impedance variation across devices. The improved programming algorithm achieves more consistent path resistances across a population of UT6325 devices that are programmed with identical designs.

**Background:**

As part of its continuous product improvement efforts, a team of product, test, quality, reliability, design, and applications engineers from Aeroflex and Quicklogic Inc. have studied and evaluated methods to improve post-programmed ViaLink quality. The findings of this study indicated that a minor change in the number of programming pulses defined in the QL9600 programming driver for the UT6325 will significantly improve the consistency of path resistances on UT6325 devices programmed with identical designs comparing the old and new methodologies.

The original UT6325 programming driver (release 1.32D) employed the same programming algorithm that Quicklogic Inc. uses with its Eclipse family of FPGAs. This algorithm groups ViaLinks into four categories based upon the design implementation and/or net loading associated with the respective links. Default and lightly-loaded ViaLinks receive fewer programming pulses than moderate and heavily-loaded nets. When comparing ViaLink impedances across multiple UT6325 devices, the Aeroflex/Quicklogic study found that default and lightly-loaded ViaLinks presented a distinct increase in ViaLink impedance variation when compared to variation measurements taken from the moderate and heavily-loaded categories.

Recognizing the correlation between ViaLink categories and the resulting consistency of ViaLink impedance across programmed devices, Aeroflex and Quicklogic instituted the QL9600 programming driver 1.32G. The new driver groups all ViaLinks into the moderate and heavily-loaded categories when deciding how many programming pulses to apply on each ViaLink. This provides reduced variation of the impedance in the default and lightly-loaded ViaLink categories. No other changes are made to the device programming driver (e.g. current clamping, voltage amplitude, programming pulse width, etc.) The comparative results of the 1.32D and new 1.32G QL9600 programming driver are depicted in Table 1.

**Table 1. Programming Algorithm Comparison of ViaLink Tolerance to Nominal Resistive Values Measured for Identical Links on Multiple Devices**

	Default ViaLink		User Lightly Loaded ViaLink		User Moderately Loaded ViaLink		User Heavily Loaded ViaLink	
	Algorithm 1.32D	Algorithm 1.32G	Algorithm 1.32D	Algorithm 1.32G	Algorithm 1.32D	Algorithm 1.32G	Algorithm 1.32D	Algorithm 1.32G
% Tolerance to Nominal Link Resistance								
+/-5%	78.567%	91.494%	82.623%	98.678%	83.739%	98.665%	83.154%	99.176%
+/-10%	97.888%	99.366%	99.545%	99.956%	99.569%	99.964%	99.702%	99.995%
+/-15%	99.813%	99.983%	99.973%	99.999%	99.915%	100.000%	99.977%	100.000%
+/-20%	99.940%	99.999%	99.993%	100.000%	99.959%	100.000%	99.991%	100.000%

n(1.32D) = 14,932,068 fuses measured

n(1.32G) = 326,384 fuses measured

**Summary:**

To date, Aeroflex has completed failure-free stress tests exceeding 926,622 device hours of High-Temperature Operating Life (HTOL) and 1,132,588 device hours of Low-Temperature Operating Life (LTOL) using UT6325 devices programmed with the 1.32D algorithm. Since programming algorithm 1.32G uses an optimal subset of the programming resources found in 1.32D, the historical device stress results are applicable to devices programmed with QL9600 programming driver 1.32G. Furthermore, Aeroflex has accumulated more than 6000 device hours of HTOL stress using programming algorithm 1.32G to verify that the new programming algorithm is compatible with the 1.32D from a reliability standpoint.

The 1.32G QL9600 programming driver is downloadable on the following Aeroflex FTP site link:  
[ftp://ftp.utmc.com/ut6325\\_radhard\\_eclipse/system\\_general\\_QL9600/system\\_general\\_132g/132G.zip](ftp://ftp.utmc.com/ut6325_radhard_eclipse/system_general_QL9600/system_general_132g/132G.zip)

Because the programming algorithm 1.32G averages more programming pulses to individual links than 1.32D, the user should expect a slight increase in programming time. Aeroflex reliability designs, for example, have increased from approximately 35 minutes to 45 minutes per device.

If you have any questions regarding the UT6325 or the QL9600 Programming Driver version 1.32G, please call or email Ron Lake at 719-594-8491 ([lake@aeroflex.com](mailto:lake@aeroflex.com)).

Regards,

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