REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Increase total dose for device 01 through 04 in 1.5. Correct dimension e for case outline Y. phn	04-09-01	Thomas M. Hess
B	Add 2.5 V configuration to the absolute maximum rating in 1.3 and recommended operating conditions in 1.4. Additional tests for 2.5 V in table I. Correct errors in case X and Y dimensions. - phn	05-06-22	Thomas M. Hess
C	Correct dimensions for case outline X. . Correct the wording “Accelerated annealing testing” in section 4.4.4.1.1 for RHA device testing. - phn	07-02-26	Thomas M. Hess
D	Device type 14 and 15 are no longer available. Updated “Radiation features”, in section 1.5. - phn	10-07-12	Thomas M. Hess

REV	D	D	D	D	D	D
SHEET	15	16	17	18	19	20

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
04-08-06

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, GATE ARRAY, RADIATION HARDENED, MONOLITHIC SILICON

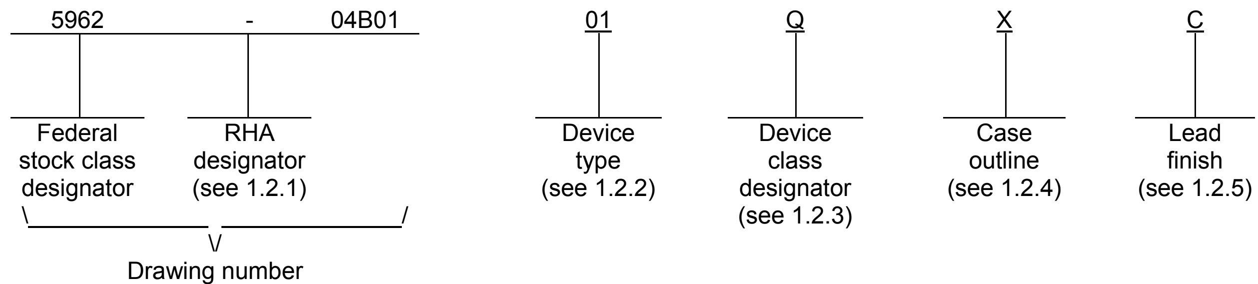
SIZE	CAGE CODE	
A	**67268**	**5962-04B01**

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Signal I/O 2/	Power & Ground Pads 3/
01	06MRA010	10,000 gates available	58	6
02	06MRA025	25,000 gates available	192	48
03	06MRA050	50,000 gates available	192	48
04	06MRA075	75,000 gates available	308	76
05	06MRA100	100,000 gates available	308	76
06	06MRA150	150,000 gates available	308	76
07	06MRA200	200,000 gates available	432	96
08	06MRA250	250,000 gates available	432	96
09	06MRA300	300,000 gates available	432	96
10	06MRA350	350,000 gates available	432	96
11	06MRA400	400,000 gates available	544	144
12	06MRA450	450,000 gates available	544	144
13	06MRA500	500,000 gates available	544	144
14	06MRA550 4/	550,000 gates available	544	144
15	06MRA600 4/	600,000 gates available	544	144

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1/ These devices are capable of being configured and support dual voltage: 3.3 V core / 3.3 V and/or 5 V bus, 5 V core/5 V bus. The supply voltage range shall be specified in the AID.
2/ Includes 5 pins that may or may not be reserved for JTAG boundary scan.
3/ Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.
4/ No longer available from an approved source of supply.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter 5/	Descriptive designator	Terminals	Package style
X	See figure 1	256	Ceramic quad flatpack
Y	See figure 1	208	Ceramic quad flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 6/

DC supply voltage (V_{DD})
- 2.5 Volt configuration (V_{DDC} only) .... -0.3 V to 3.0 V
- 3.3 Volt configuration (V_{DDC} only) .... -0.3 V to 3.9 V
- 5.0 Volt configuration (V_{DDC} only) .... -0.3 V to 6.0 V

Voltage on any pin ($V_{I/O}$) 7/
- 3.3 Volt configuration .... -0.3 V to V_{DD} + 0.3 V
- 5.0 Volt configuration .... -0.3 V to V_{DD} + 0.3 V

Storage temperature (T_{STG}) .... -65°C to +150°C

Maximum junction temperature (T_J) .... +175°C

Latchup immunity (I_{LU}) .... ±150 mA

DC input current (I_I) .... ±10 mA

Lead Temperature (soldering 5 sec) .... +300°C

1.4 Recommended operating conditions.

Positive supply voltage (V_{DD})
- 3.3 Volt configuration ($V_{I/O}$ and V_{DDC}) .... +3.0 V to +3.6 V
- 5.0 Volt configuration ($V_{I/O}$ and V_{DDC}) .... +4.5 V to +5.5 V

DC input voltage (V_{IN}) .... 0 V to V_{DD}

Case temperature range (T_C) .... -55°C to +125°C

1.5 Radiation features.

Total dose:
- For device 01 through 04 (Dose rate = 50 – 300 Rad(Si)/s) .... ≥ 3 x 10^5 Rads (Si) 8/
- For device 05 through 15 (Dose rate = 50 – 300 Rad(Si)/s) .... ≥ 1 x 10^5 Rads (Si) 8/

Single event phenomenon (SEP) effective
- LET, no upset 9/
- LET, no latchup .... ≥ 109 MeV-cm^2/mg

Dose rate upset (20 ns pulse) .... ≥ 4.4 x 10^8 Rad(Si)/s @ 4.5 V_{DD} 10/

Dose rate latchup .... ≥ 3.8 x 10^{11} Rad(Si)/s 10/

Dose rate Survivability .... ≥ 3.8 x 10^{11} Rad(Si)/s 10/

Neutron irradiated .... ≥1 x 10^{14} neutron/cm^2

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) .... as specified in the AID

______

5/ Additional packages are available on SMD 5962-99B01.

6/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

7/ For cold spare mode (V_{DD} = V_{SS}), $V_{I/O}$ would be ± 0.3 V to maximum recommended operating condition.

8/ The dose rate shall be 50 – 300 Rad(Si)/s unless otherwise specified in the AID.

9/ When characterized as a result of the procuring activities request, the condition will be specified.

10/ Applicable to ON Semi Fab 9 fabricated material.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
MIL-PRF-55681 - Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, General Specification for.
MIL-PRF-123 - Capacitors, Fixed, Ceramic Dielectric, (Temperature Stable and General Purpose), High Reliability, General Specification for

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 – IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and as specified in figure 1.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent HDL behavioral description).

3.3.4 Functional description terms and symbols.

3.3.5 Logic diagram (or equivalent structural HDL description or mutually agreed to net list).

3.3.6 Pin function description.

3.3.7 Design tape # or Design document name (i.e., net list).

3.3.8 Design functional tape # or name.

3.3.9 Test functional tape # or name.

3.3.10 Timing diagram(s).

3.3.11 Fault coverage measurement of manufacturing logic tests.

3.3.12 Burn-in circuit.

3.3.13 ESD class and voltage.

3.3.14 Device electrical performance characteristics (additions to Table I). Device electrical performance characteristics shall include dc parametric, functional, ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.15 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.16 Supply voltage range. The supply voltage range shall be as specified in the AID.

3.3.17 Dose rate. The dose rate shall be 50 – 300 Rad(Si)/s depending on total dose requirement unless otherwise specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_C ≤ +125°C V_{DD} = 5.0 V ± 10% V_{DDC} = 5.0/3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low-level input voltage	V_{IL}	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All			V
TTL inputs						0.8	
CMOS inputs 3/						0.3V_{DD}	
High-level input voltage	V_{IH}	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All			V
TTL inputs					2.2		
CMOS inputs 3/					0.7V_{DD}		
Schmitt Trigger, positive going threshold 3/	V_T+	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All			V
TTL						2.4	
CMOS						0.7V_{DD}	
Schmitt Trigger, negative going threshold 3/	V_T-	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All			V
TTL					0.9		
CMOS					0.3V_{DD}		
Schmitt Trigger, typical range of hysterisis 4/	V_H		1, 2, 3	All			V
TTL					0.4		
CMOS					0.6		
Input leakage current	I_{IN}	V_{DD} = 5.5 V					
TTL, CMOS and Schmitt inputs		V_{IN} = V_{DD} and V_{SS}	1, 2, 3	All	-1	1	µA
Inputs with pull-down resistors		V_{IN} = V_{DD}			20	225	
Inputs with pull-down resistors		V_{IN} = V_{SS}			-5	5	
Inputs with pull-up resistors		V_{IN} = V_{SS}			-225	-20	
Inputs with pull-up resistors		V_{IN} = V_{DD}			-5	5	
Cold spare inputs – “Off”		V_{IN} = 0 to 5.5 V			-5	5	
Cold spare inputs – “On”		V_{DDC} = V_{DD} = V_{SS} = 0 V V_{IN} = 0 V and 5.5 V			-5	5	
Low-level output voltage	V_{OL}	V_{DD} = 4.5 V	1, 2, 3	All			
TTL 2.0 mA buffer		I_{OL} = 2.0 mA				0.4	V
TTL 4.0 mA buffer		I_{OL} = 4.0 mA				0.4	
TTL 8.0 mA buffer		I_{OL} = 8.0 mA				0.4	
TTL12.0 mA buffer		I_{OL} = 12.0 mA				0.4	
CMOS outputs		I_{OL} = 1.0 µA				0.05	
CMOS outputs (Optional)		I_{OL} = 100.0 µA				0.25	
CMOS outputs (Cold spare)		I_{OL} = 100.0 µA				0.25	
High-level output voltage	V_{OH}	V_{DD} = 4.5 V	1, 2, 3	All			
TTL 2.0 mA buffer		I_{OH} = -2.0 mA			2.4		V
TTL 4.0 mA buffer		I_{OH} = -4.0 mA			2.4		
TTL 8.0 mA buffer		I_{OH} = -8.0 mA			2.4		
TTL12.0 mA buffer		I_{OH} = -12.0 mA			2.4		
CMOS outputs		I_{OH} = -1.0 µA			V_{DD} – 0.05		
CMOS outputs (Optional)		I_{OH} = -100.0 µA			V_{DD} – 0.35		
CMOS outputs (Cold spare)		I_{OH} = -100.0 µA			V_{DD} – 0.35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_C \leq +125°C$ V_{DD} = 5.0 V ± 10% V_{DDC} = 5.0/3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Three-state output leakage current TTL 2.0 mA buffer TTL 4.0 mA buffer TTL 8.0 mA buffer TTL12.0 mA buffer Cold spare inputs – "Off" Cold spare inputs – "On"	I_{OZ}	V_{DD} = 5.5 V V_O = 0 V and 5.5 V $V_{DDC} = V_{DD} = V_{SS}$ = 0 V V_O = 0 V and 5.5 V	1, 2, 3	All	 -5 -10 -20 -30 -5 -5	 5 10 20 30 -5 -5	μA
Short-circuit output current 4/ 5/ TTL 2.0 mA buffer TTL 4.0 mA buffer TTL 8.0 mA buffer TTL12.0 mA buffer	I_{OS}	V_O = 0 V and 5.5 V	1, 2, 3	All	 -50 -100 -200 -300	 50 100 200 300	mA
Quiescent supply current 6/	I_{DDQ}	V_{DDC} = 5.5 V 200K gates 400K gates 600K gates	1,3	All		 50 100 150	μA
		V_{DDC} = 5.5 V 200K gates 400K gates 600K gates	2			 1 2 3	mA
		V_{DDC} = 5.5 V 200K gates 400K gates 600K gates — M, D, P, L, R, F	1	All		 4 8 12	mA
Quiescent supply current 6/	I_{DDQ}	V_{DDC} = 3.6 V 200K gates 400K gates 600K gates	1,3	All		 50 100 150	μA
		V_{DDC} = 3.6 V 200K gates 400K gates 600K gates	2			 1 2 3	mA
		V_{DDC} = 3.6 V 200K gates 400K gates 600K gates — M, D, P, L, R, F	1	All		 4 8 12	mA

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_C \leq +125°C$ V_{DD} = 5.0 V ± 10% V_{DDC} = 5.0/3.3 V ± 10% unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input capacitance 7/	C_{IN}		4	All			23	pF
Output capacitance 7/								
TTL 2.0 mA buffer	C_{OUT}		4	All			22	pF
TTL 4.0 mA buffer							26	
TTL 8.0 mA buffer							26	
TTL12.0 mA buffer							26	
Bidirect I/O capacitance 7/								
TTL 4.0 mA buffer	C_{IO}		4	All			24	pF
TTL 8.0 mA buffer							26	
TTL12.0 mA buffer							26	

See notes at end of table

TABLE I. Electrical performance characteristics – Continued..

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_C \leq +125°C$ V_{DD} = 3.3 V ± 10% V_{DDC} = 3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low-level input voltage CMOS inputs 3/	V_{IL}	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All		$0.3V_{DD}$	V
High-level input voltage CMOS inputs 3/	V_{IH}	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All	$0.7V_{DD}$		V
Schmitt Trigger, positive going threshold, CMOS 3/	V_T+	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All		$0.7V_{DD}$	V
Schmitt Trigger, negative going threshold, CMOS 3/	V_T-	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All	$0.3V_{DD}$		V
Schmitt Trigger, typical range of hysterisis, CMOS 4/	V_H		1, 2, 3	All	0.6		V
Input leakage current	I_{IN}	V_{DD} = 3.6 V	1, 2, 3	All			µA
CMOS and Schmitt inputs		$V_{IN} = V_{DD}$ and V_{SS}			-1	1	
Inputs with pull-down resistors		$V_{IN} = V_{DD}$			10	225	
Inputs with pull-down resistors		$V_{IN} = V_{SS}$			-5	5	
Inputs with pull-up resistors		$V_{IN} = V_{SS}$			-225	-10	
Inputs with pull-up resistors		$V_{IN} = V_{DD}$			-5	5	
Cold spare inputs – “Off”		V_{IN} = 0 to 3.6 V			-5	5	
Cold spare inputs – “On”		$V_{DDC} = V_{DD} = V_{SS}$ = 0 V V_{IN} = 0 V and 3.6 V.			-5	5	
Low-level output voltage	V_{OL}		1, 2, 3	All			V
CMOS outputs		I_{OL} = 1.0 µA				0.05	
CMOS outputs (Optional)		I_{OL} = 100.0 µA				0.25	
CMOS outputs (cold spare)		I_{OL} = 100.0 µA				0.25	
High-level output voltage	V_{OH}		1, 2, 3	All			V
CMOS outputs		I_{OH} = -1.0 µA			V_{DD} – 0.05		
CMOS outputs (Optional)		I_{OH} = -100.0 µA			V_{DD} – 0.35		
CMOS outputs(cold spare)		I_{OH} = -100.0 µA			V_{DD} – 0.35		
Three-state output leakage current	I_{OZ}	V_{DD} = 3.6 V	1, 2, 3	All			µA
CMOS		$V_O = V_{DD}$ and V_{SS}			-20	20	
Cold spare inputs – “Off”		V_O = 0 V and 3.6 V			-5	5	
Cold spare inputs – “On”		$V_{DDC} = V_{DD} = V_{SS}$ = 0 V $V_{IN} = V_{DD}$ or V_{SS}			-5	5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_C \leq +125°C$ V_{DD} = 3.3 V ± 10% V_{DDC} = 3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Short-circuit output current 4/ 5/ CMOS	I_{OS}	V_O = 0 V and 3.6 V	1, 2, 3	All	-200	200	mA
Quiescent supply current 6/	I_{DDQ}	V_{DDC} = 3.6 V 200K gates 400K gates 600K gates	1,3	All		50 100 150	µA
		V_{DDC} = 3.6 V 200K gates 400K gates 600K gates	2			1 2 3	mA
		V_{DDC} = 3.6 V 200K gates 400K gates 600K gates M, D, P, L, R	1			4 8 12	mA
Input capacitance 7/	C_{IN}		4	All		23	pF
Output capacitance, CMOS 7/	C_{OUT}		4	All		26	pF
Bidirect I/O capacitance, CMOS 7/	C_{IO}		4	All		26	pF

Notes:

1/ These devices are capable of being configured and support dual voltage: 3.3 V core/ 3.3 V and /or 5.0 V bus, 2.5 V core/3.3 V or 5.0 V bus, or 5 V core/5 V bus. The supply voltage range shall be specified in the AID.

2/ Devices supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation. However, this device is only tested at the 'R' or 'F' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25 C.

3/ Functional tests are conducted in accordance with MIL-STD-883 with the following input conditions:
$V_{IH} = V_{IH}(min)$ + 20%, - 0%; $V_{IL} – V_{IL}(max)$ +0%, -50%, as specified herein for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

4/ Supplied as a design limit but not guaranteed or tested.

5/ Not more than one output may be shorted at a time for maximum duration of one second.

6/ All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

7/ Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1 MHz @ 0 V and a signal amplitude of ≤ 50 mV RMS

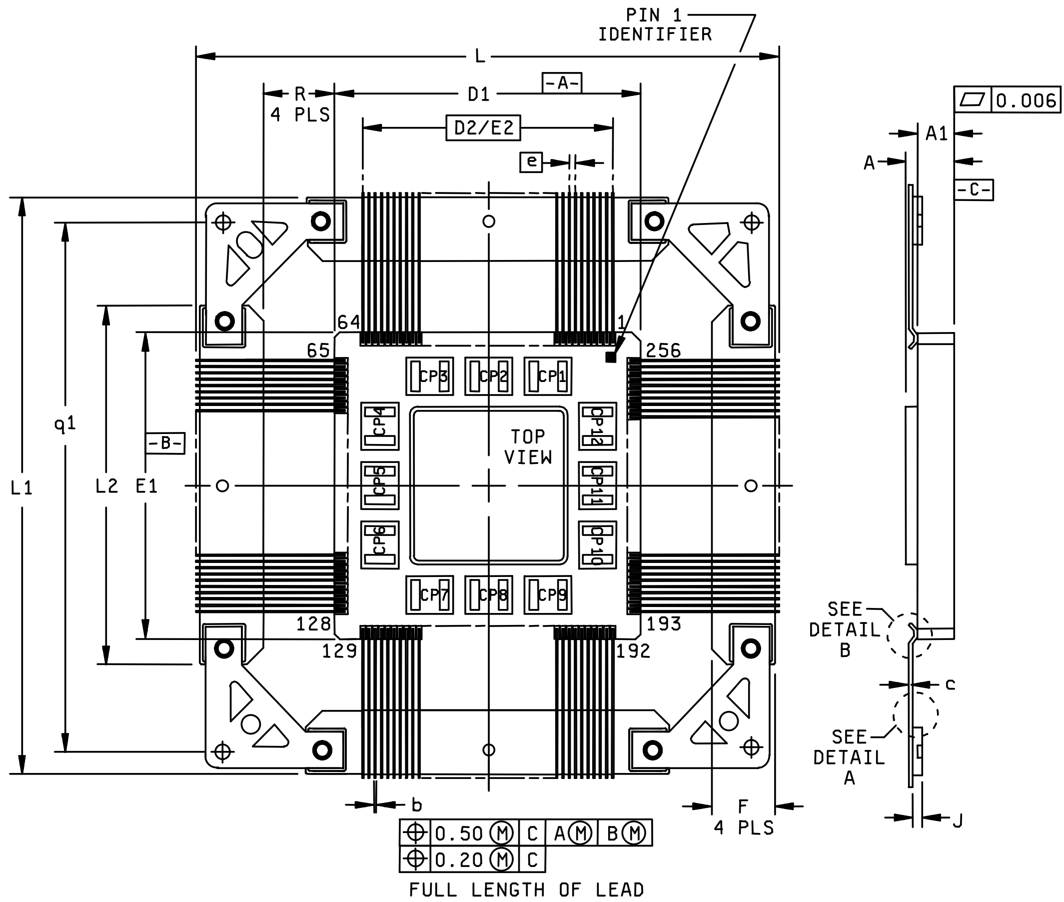
TABLE IB. SEP test limits . 1/ 2/

Device Type	T_A = Temperature ±10°C	SEU BIAS, V_{CC} = 4.5 V, 3.0 V		Bias for latch-up test V_{CC} = 5.5 V,
		Effective LET no upsets [MEV – cm^2/mg]	Maximum device cross section (μm^2) (LET = 120)	No latch-up LET
All	3/	4/	4/	≥ 109 Mev – mg/cm^2

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A.

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature for latch up test T_A = +125°C; . worst case temperature for set up test T_A = +25°C for SEU test.
4/ When characterized as a result of the procuring activities request, this parameter will be specified.

Case X



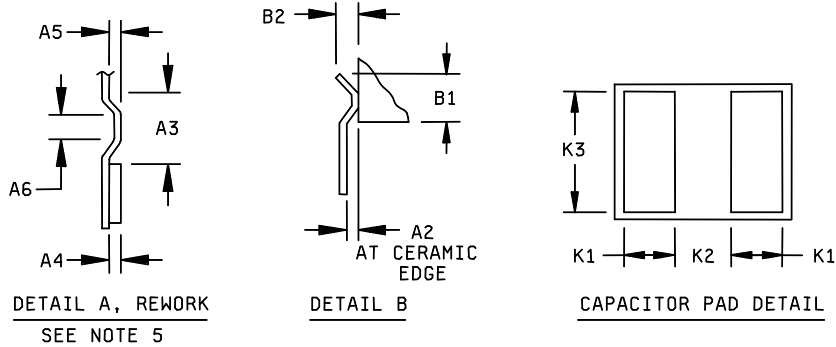


FIGURE 1. Case outline.

Case X - Continued

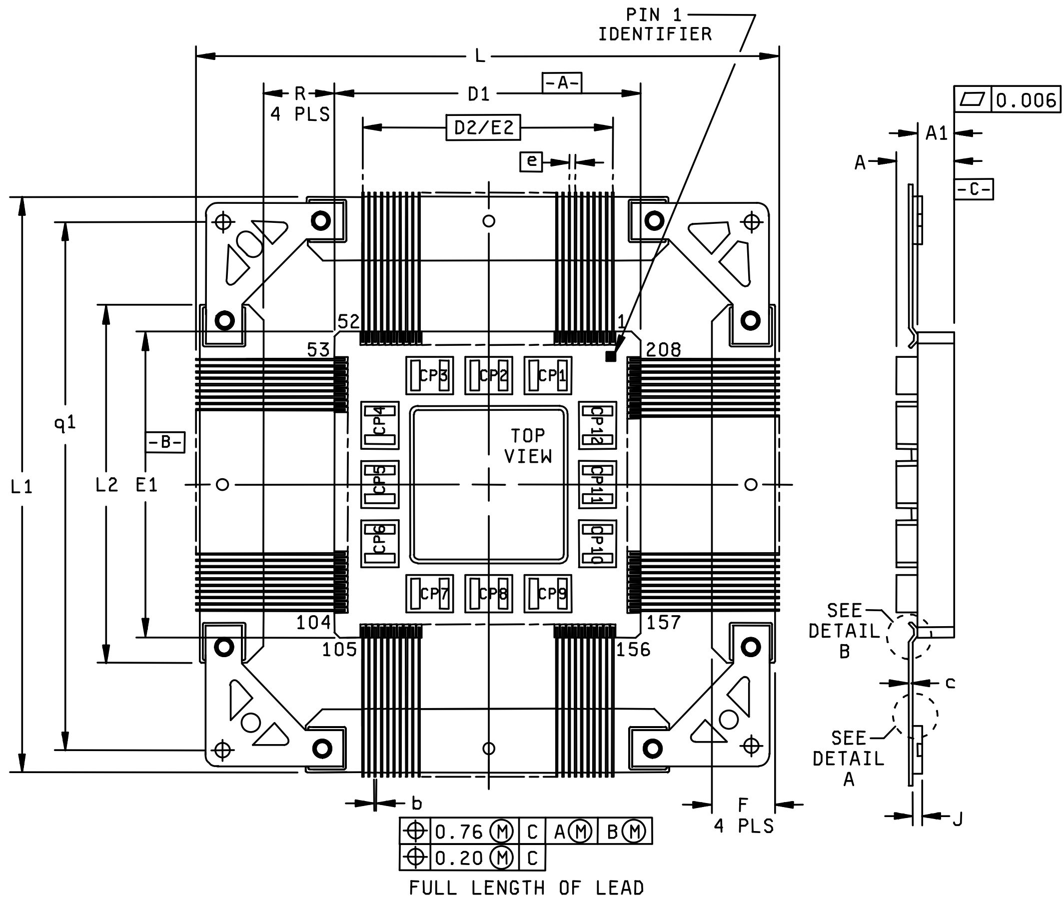
CP1	V_{DDCQ}	CP5	V_{DD1}	CP9	V_{DD1}
CP2	V_{DDNCQ}	CP6	V_{DD1}	CP10	V_{DD1}
CP3	V_{DD1}	CP7	V_{DD1}	CP11	V_{DD1}
CP4	V_{DD1}	CP8	V_{DD1}	CP12	V_{DDCQ}

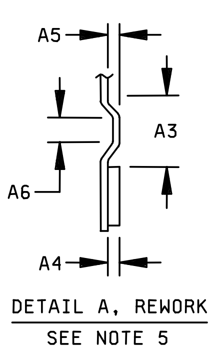
Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		3.81		.150	F		8.56		.337
A1		3.18		.125	D1/E1	35.64	36.70	1.403	1.445
A2	0.15	0.30	.006	.012	D2/E2	31.50 BSC		1.240 BSC	
A3		1.90		.075	L		77.21		3.040
A4	0.89 REF		.035 REF		L1		75.39		2.968
A5		0.89		.035	L2	56.31 REF		2.217 REF	
A6	1.27 REF		.050 REF		K1	1.52		.060	
B1		1.65		.065	K2	2.54		.100	
B2		0.46		.018	K3	3.56		.140	
b	0.13	0.25	.005	.010	q1	70.00 REF		2.756 REF	
c	0.10	0.20	.004	.008	J	0.77	1.03	.030	.040
e	0.50 BSC		.019 BSC						

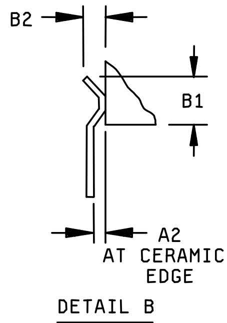
Notes:
1. All exposes metalized areas are gold plated over nickel plating per MIL-PRF-38535.
2. The lid is connected to V_{SS}.
3. Capacitors pads are designed for a MIL-PRF-55681 CDR33BX, 50V .1μF chip cap.
4. Tiebar areas may have notches and tabs different than shown.
5. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired areas.

FIGURE 1. Case outline - Continued.

Case Y







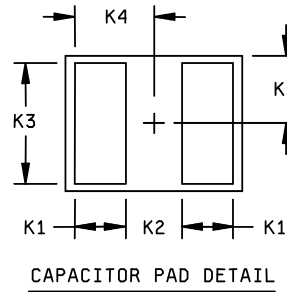


FIGURE 1. Case outline - Continued.

Case Y - Continued

CP1	V_{DD1}	CP5	V_{DDCQ}	CP9	V_{DD1}
CP2	V_{DDCQ}	CP6	V_{DD1}	CP10	V_{DD1}
CP3	V_{DD1}	CP7	V_{DD1}	CP11	V_{DDCQ}
CP4	V_{DD1}	CP8	V_{DD1}	CP12	V_{DD1}

Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		4.17		.157	D1/E1	27.80	28.13	1.097	1.107
A1		2.67		.105	D2/E2	25.50 BSC		1.004 BSC	
A2		0.25		.010	L		77.22		3.040
A3		1.90		.074	L1		75.39		2.968
A4	0.89 REF		.035 REF		L2	56.31 REF		2.217 REF	
A5		0.89		.035	K1	1.40		.055	
A6	1.27 REF		.050 REF		K2	1.65		.064	
B1		0.71		.028	K3	2.79		.109	
B2		0.36		.014	K4	2.22		.087	
b	0.15	0.25	.005	.010	K5	1.40		.055	
c	0.10	0.20	.004	.008	q1	65.89 REF		2.594 REF	
e	0.50 BSC		.020 BSC		J	0.77	1.03	.030	.040
F		7.75		.306	R	29.00		.787	

Notes:

1. All exposes metalized areas are gold plated over nickel plating per MIL-PRF-38535.
2. The lid is connected to V_{SS}.
3. Capacitors pads are designed for a MIL-PRF-55681 CDR33BX, 50V .1µF chip cap.
4. Tiebar areas may have notches and tabs different than shown.
5. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired areas.

FIGURE 1. Case outline - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class Q and V, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as described in the AID.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for initial qualification and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND. Capacitance testing shall be performed on three devices per Method 3012. A minimum of four pins per device shall be tested. Tested pins shall be selected based on engineering analysis of the package interconnect drawing to determine which pins will have the highest capacitance. The sample sizes may be increased based on engineering judgement, but shall not be decreased.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	- - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7	1, 7	1, 7
Group D end-point electrical parameters (see 4.4)	1, 7	1, 7	1, 7
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.5 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.5). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be as specified in Table IB SEP test limits.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-07-12

Approved sources of supply for SMD 5962-04B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor Similar PIN 3/
5962F04B0101Q_C 5962F04B0101V_C	65342	UT06MRA010
5962F04B0102Q_C 5962F04B0102V_C	65342	UT06MRA025
5962F04B0103Q_C 5962F04B0103V_C	65342	UT06MRA050
5962F04B0104Q_C 5962F04B0104V_C	65342	UT06MRA075
5962R04B0105Q_C 5962R04B0105V_C	65342	UT06MRA100
5962R04B0106Q_C 5962R04B0106V_C	65342	UT06MRA150
5962R04B0107Q_C 5962R04B0107V_C	65342	UT06MRA200
5962R04B0108Q_C 5962R04B0108V_C	65342	UT06MRA250
5962R04B0109Q_C 5962R04B0109V_C	65342	UT06MRA300
5962R04B0110Q_C 5962R04B0110V_C	65342	UT06MRA350
5962R04B0111Q_C 5962R04B0111V_C	65342	UT06MRA400
5962R04B0112Q_C 5962R04B0112V_C	65342	UT06MRA450
5962-04B0113Q_C 5962R04B0113V_C	65342	UT06MRA500
5962-04B0114Q_C 5962R04B0114V_C	4/	UT06MRA550
5962-04B0115Q_C 5962R04B0115V_C	4/	UT06MRA600

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Due to the nature of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID. The vendor similar PIN will be based on the UT06MRA gate array family. Contact the listed approved source of supply for availability of case outlines (defined in 1.2.4) for each device.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

4/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.