

QML Gate Array Program



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INTRODUCTION

Aeroflex UTMC is the first manufacturer to achieve DSCC certification and qualification to build CMOS gate arrays to the generic family qualification requirements defined in the military device specifications. Qualification has been extended to include QML Class Q and V on the 0.6 μ and 0.25 μ gate array families. The certified design system and process controls assure the entire product family consistently meets the quality and reliability requirements for military and defense applications. Therefore, the customer can buy QML product for gate array designs without expending the added time and expense of qualifying each design personalization.

Qualified QML gate array designs are eligible for listing in Goddard Space Flight Center Preferred Parts List PPL.

The QML gate array program allows the customer to define the application-specific design requirements in the customer's own Altered Item Drawing (AID). This drawing defines electrical performance requirements for the specific application in addition to the minimum static (DC) tests defined in the QML device specification. Thus the customer maintains control over the device design. The AID drawing simply refers to the applicable QML device specification for all quality requirements, eliminating the costs of developing a source control drawing to define special qualification and technology conformance inspection requirements.

Altered Item Drawing (AID) Requirements

The customer controls the design details by defining the application-specific requirements completely within the AID. The AID does not alter the standard microcircuit drawing requirements but supplements the requirements by defining additional electrical test and design requirements for the specific application. There is no need to specify the construction, quality, and reliability requirements in the AID as these are covered in Standard Microcircuit Drawing 5962-96B02, 5962-97B04 and 5962-99B01. This benefits the customer in not having to negotiate special quality clauses in a source control drawing

(SCD). The customer submits the AID drawing to Aeroflex UTMC to establish contractual agreement on the design and to confirm that the AID meets the requirements of the QML gate array slashesheets. As an option, Aeroflex UTMC can prepare the customer's AID, further streamlining the procurement process.

The following list outlines the AID requirements.

- Functional description, terms, and symbols
- Terminal connections and pin assignments
- Package type qualified on QML-38535 (Contact Aeroflex UTMC for the current qualification information)
- Functional block diagram
- Logic diagram; pin function description
- Schematic circuits
- Test vectors including fault grading percentage of detectable stuck-at-0 and stuck-at-1 faults (Aeroflex UTMC will supply fault grading results to customer for inclusion to the AID)
- Device electrical performance characteristics; static (including static electricals per slashesheet), functional, and switching critical paths
- Critical timing diagrams; burn-in circuit
- Maximum power dissipation
- Total dose bias circuit (if applicable)

Aeroflex UTMC has developed an AID boilerplate format to help customers generate their drawings more rapidly. Contact Aeroflex UTMC to obtain the AID format.