Application Note

ACT 5028 Resolver-To-Digital Converter

Dose-Rate Testing of the Resolver-to-Digital Converter

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August 2003

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Introduction

This document reports on the test method used and the results obtained in tests exposing the MRC/Aeroflex Resolver-to-Digital Converter designed by TAG. The development and qualification of this design has been funded by the Navy under contracts N00164-02-D-6599, N00164-97-D-0013, and N00164-97D-0014/0012 and /0030. Program plans do not specify a dose-rate requirement, but STSS (formerly SBIRS-Low), the original target application, and AEHF both have dose-rate environment requirements. Early RDC designs were targeted for the BAE 0.5um process with thin epi, and it was this thin epi that was originally expected to provide sufficient dose-rate tolerance without significant design effort. Subsequent design modifications, retargeted to a different process (UTMC/AMI C6N), made no further modifications to the design to specifically mitigate dose-rate effects. Latch-up immunity at dose rates of around 1e10 rad(Si)/s was adopted as a "rule-of-thumb" guideline for the performance of this chip. As our results show, the current design does not achieve this level. This report identifies the latch-up weakness in the design and describes the fixes that are being implemented in the next design.

Dose-Rate Test Setup and Method

Radiation Source:

The radiation source was the Crane LINAC. Thermo-luminescent dosimeters were used to calibrate the LINAC dose rates against current pulses on a PIN diode placed directly in front of the test RDC. We used 20ns pulse widths with a range of dose rates from 10^9 to about 2×10^{10} rad(Si)/s. The dosimetry calibration curve is shown in Figure 1.

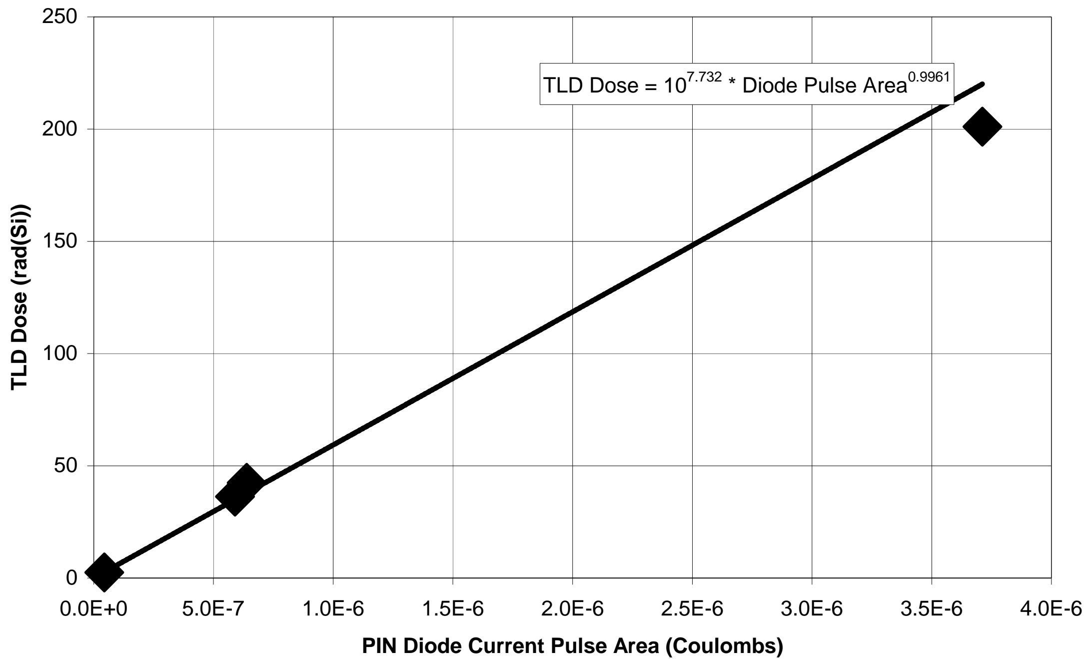

Figure 1. PIN Diode Current Pulse Width calibrated to TLD total dose.

Test Equipment:

The RDC was tested using a PC with control software driving a North Atlantic resolver simulator and reading data from the 16-bit output registers of the DUT (all testing was conducted with the part configured for 16-bit operation). Other test equipment included a manual resolver simulator, oscilloscopes, DMM's, power supplies, and a pulse counter. Lead and aluminum shielding was employed where necessary to protect these instruments. A schematic of the test setup is illustrated in Figure 2.

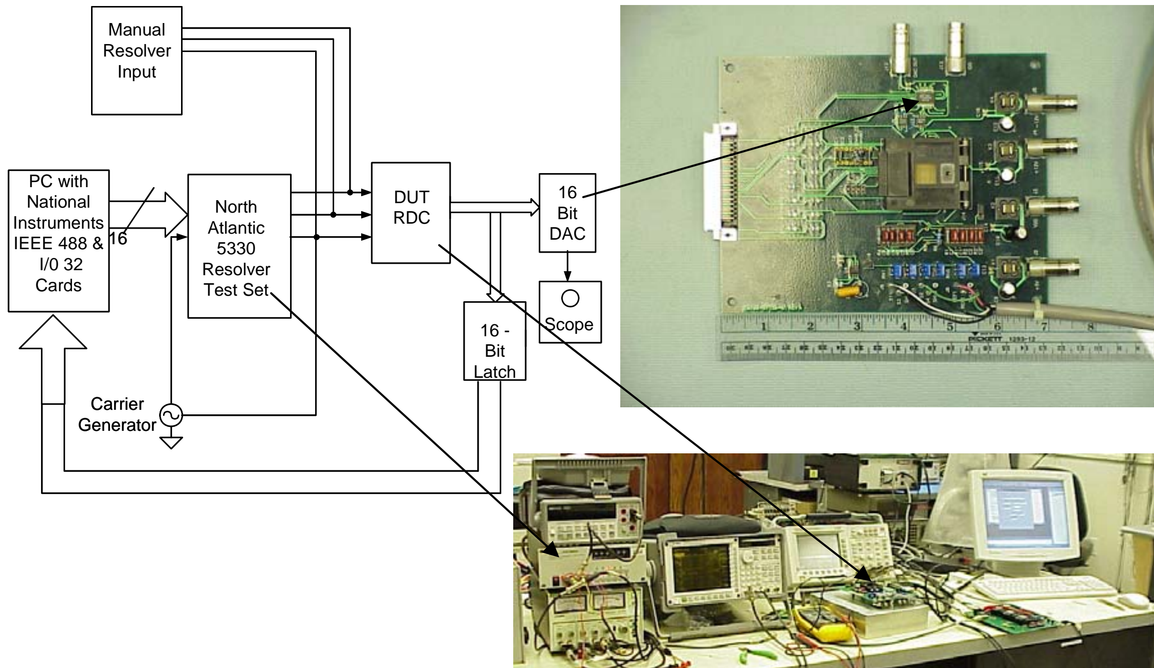

Figure 2. RDC Test Setup.

Test Devices

The ACT5028 (JY04A) version of the Resolver-to-Digital converter was tested. This part was manufactured in the AMI C6N 0.5um process with the Aeroflex UTMC rad hard process modifications for total ionizing dose hardness. Several parts were fitted with ceramic strip heaters and thermocouples for temperature control and monitoring. The test board had passive filter circuits configured for the 16-bit mode of operation. An on-board linear DAC was available on the board for monitoring output registers, but this device is near the edge of the board, out of the range of the expected diameter of the beam, and was not used in these tests. Instead, the output registers were read directly by the CPU running Visual Basic controlling a DIO-32 card. Rail-stiffening capacitors were added to the board to prevent rail-span collapse during the LINAC pulse. No power supply current limiting was employed, and drive and supply voltages were maintained at values near their set points during the pulses.

Latch-up Test Conditions

Latch-up testing was done with the RDC heated to 125C (maximum spec temp) and biased at 5.5V. These are worst-case conditions for latchup. During latch-up testing, the RDC was operated dynamically with a constantly rotating input angle. Our first tests were with relatively high dose rates. After observing latch-up at these levels, successively lower dose rates were used until no latch-up was observed. Once the range was thus bounded, finer resolution of the latch-up threshold was obtained by varying the dose-rates within this range. Dose-rate was monitored at each shot by integrating the current pulse of a PIN diode in front of the RDC.

Dose-Rate Test Results

LINAC Dose-Rate Testing at Crane was completed last month. Three parts were tested for latch-up. The latch-up thresholds ranged from 1.19e9 rad/s to 1.52e9 rad/s. No burnout was observed for these parts. When the RDC latched, it remained functional, and no parameter degradation was observed. Latch manifested itself as an increase in IDD supply current from a typical value of around 25-30mA to ~200mA. The latchup dose-rate levels are summarized in Table 1 below.

Table I. RDC Latchup Thresholds.

Part	No Latchup	Latchup
ARFLX #16	< 1.19e9	> 1.19e9
ARFLX #15	< 1.26e9	> 1.30e9
MRC #10	< 1.52e9	> 1.54e9

Using Liquid Crystal Thermal Imaging, we were able to identify the location of the latchup on the RDC chip. The hot-spot location is identified in Figure 3 below.

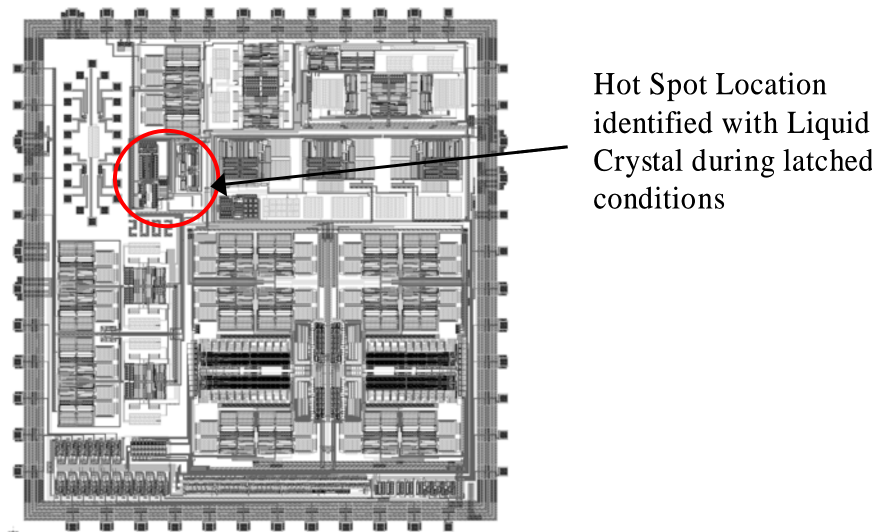

Figure 3. RDC Latchup location identified with Liquid Crystal Thermal Imaging.

The circuitry at this location is an internal amplifier that drives a large number of internal nodes. The amplifier is identified in Figure 4. Figure 5 shows the internal design of this amplifier. Note the large output transistors, M14 and M15. These transistors have W's of 300 for the NMOS M15 and 600 for the PMOS M14. The layout of these transistors is shown in Figure 6. Note the common output node metal 1 (blue) covers the entire 300um length of the adjacent guard rings. These guard rings were consequently poorly contacted, and the resistive drop was large enough to allow latch-up of the adjacent 4-layer diodes under intense photogeneration conditions. Figure 7 shows how the layout has been modified to improve the guard ring (substrate) contact density. These changes have been implemented and released to fab to improve the dose-rate-induced latch-up immunity.

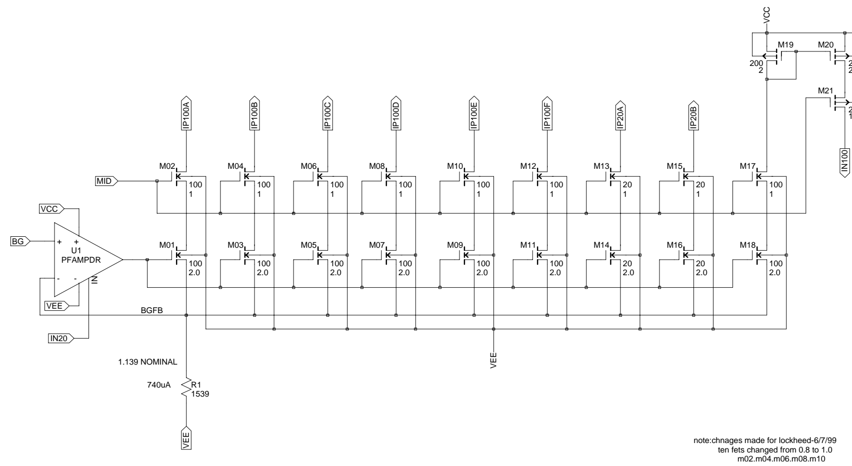

Figure 4. PFAMDR is identified as the circuit where latchup occurs.

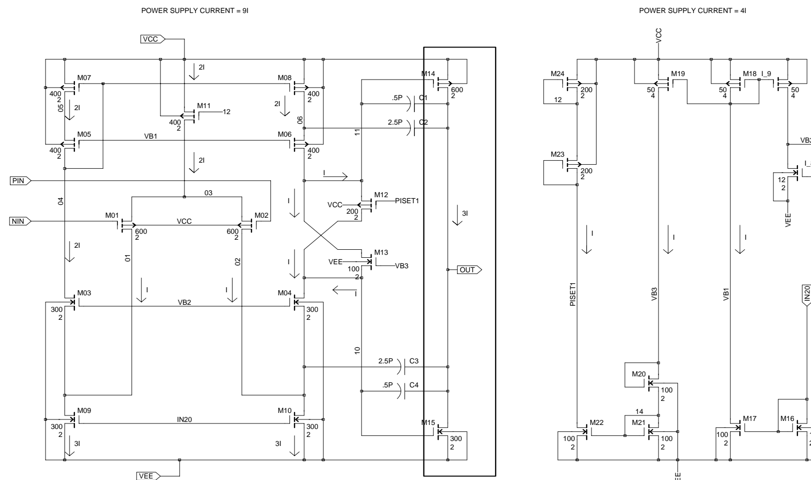

Figure 5. The large output transistors of PFAMPDR are primarily responsible for the latchup.

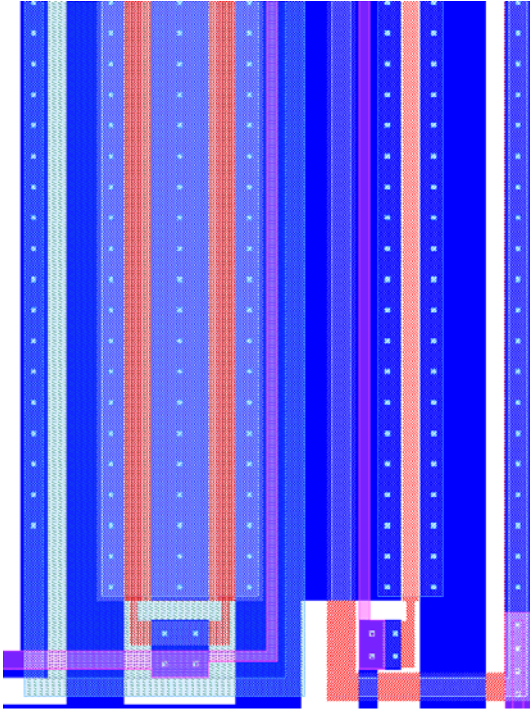

Figure 6. Layout of M14 and M15 output transistors reveals long runs of guard rings without substrate contacts

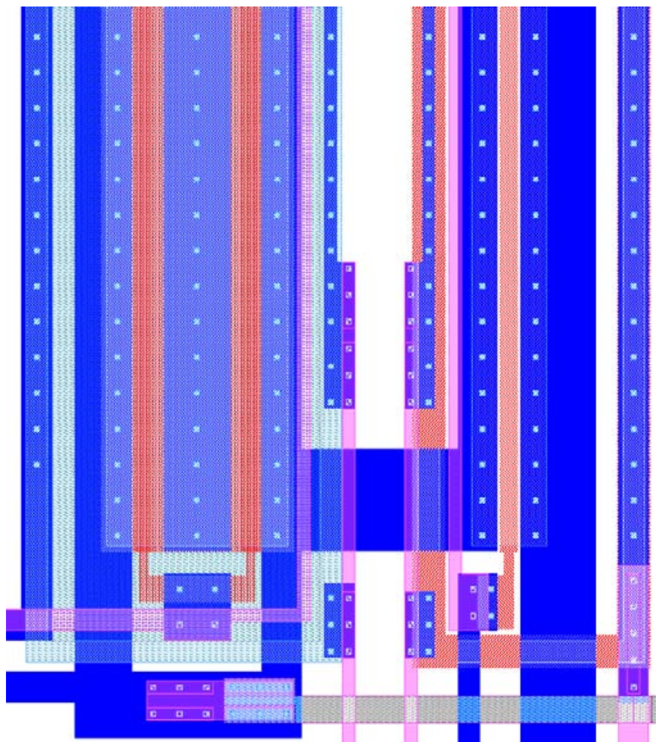

Figure 7. Layout redesign now employs sufficient substrate/guard-ring contacts to reduce the probability of latchup. Similar modifications were made chip-wide.

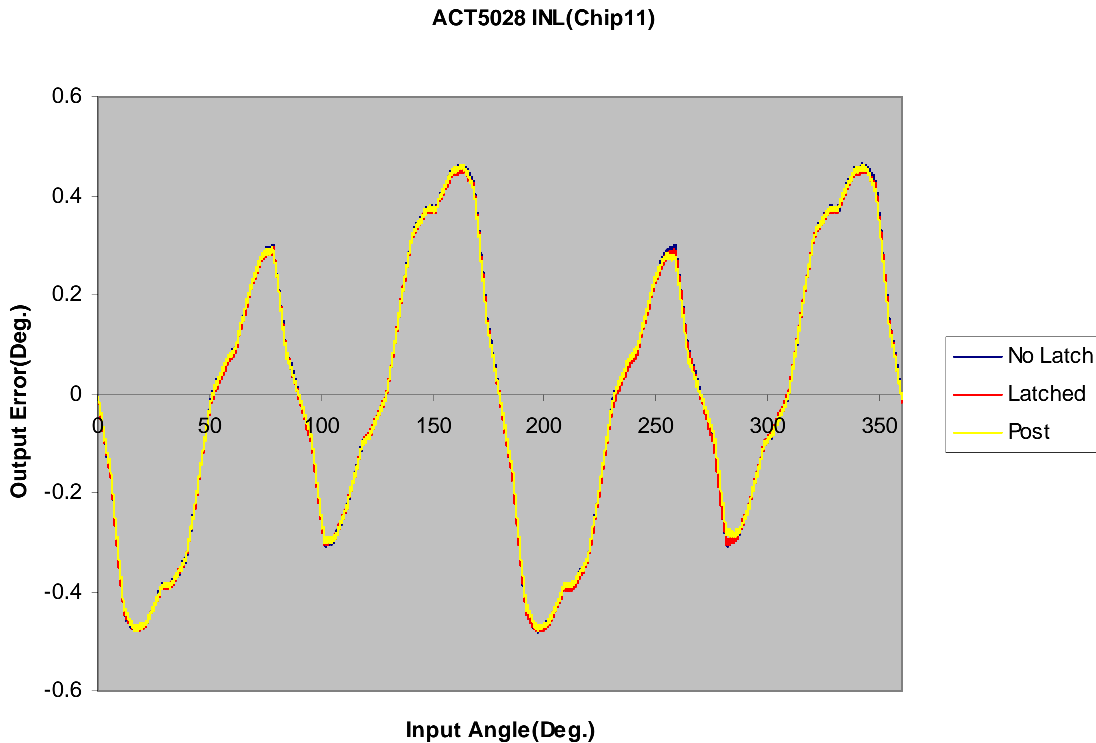

Figure 8. INL curves pre-, during, and post- latch-up.

The observed latch-up of the RDC does not lead to burn-out of the parts, and produces no degradation in device performance (INL), even during latched conditions. This is illustrated in Figure 8, where the INL curve for an example part prior to a latch-up event is compared to the INL curve after (post) the latch-up event. In addition, while the part was latched (drawing high power supply current, but otherwise functional), the INL curve was measured. (This required the part to operate in latched mode for 10 minutes or more.) All three curves are nearly identical, and do not vary significantly from typical INL curves for the RDC. In fact the differences are on the order of 1 to 3 LSB's, and are easily attributable to noise and repeatability problems in the measurements.

In addition, we have exposed several parts to energetic neutrons in the White Sands Nuclear Reactor Facility. Neutrons are known to cause bulk displacement damage in silicon, and as a result often kill parasitic lateral PNP current gain (through recombination at the displacement defect sites). This is sometimes helpful in eliminating latch-up paths. Our neutron test results show no significant effects on the performance of the RDC, suggesting the design is sufficiently hard in neutron environments to fluence levels of at least 5e13 neutrons/cm^2. These results are illustrated in Figure 9, where the approximate change in bandgap current with neutron fluence is shown. The bandgap reference circuit uses a lateral PNP, but is designed to operate even without significant gain in the PNP transistor. As a result, there is virtually no detectable change in circuit performance. However, we have observed that the parts that received neutron fluences of 5e12 neutrons/cm^2 or higher did become latch-up immune at room temperature (though they

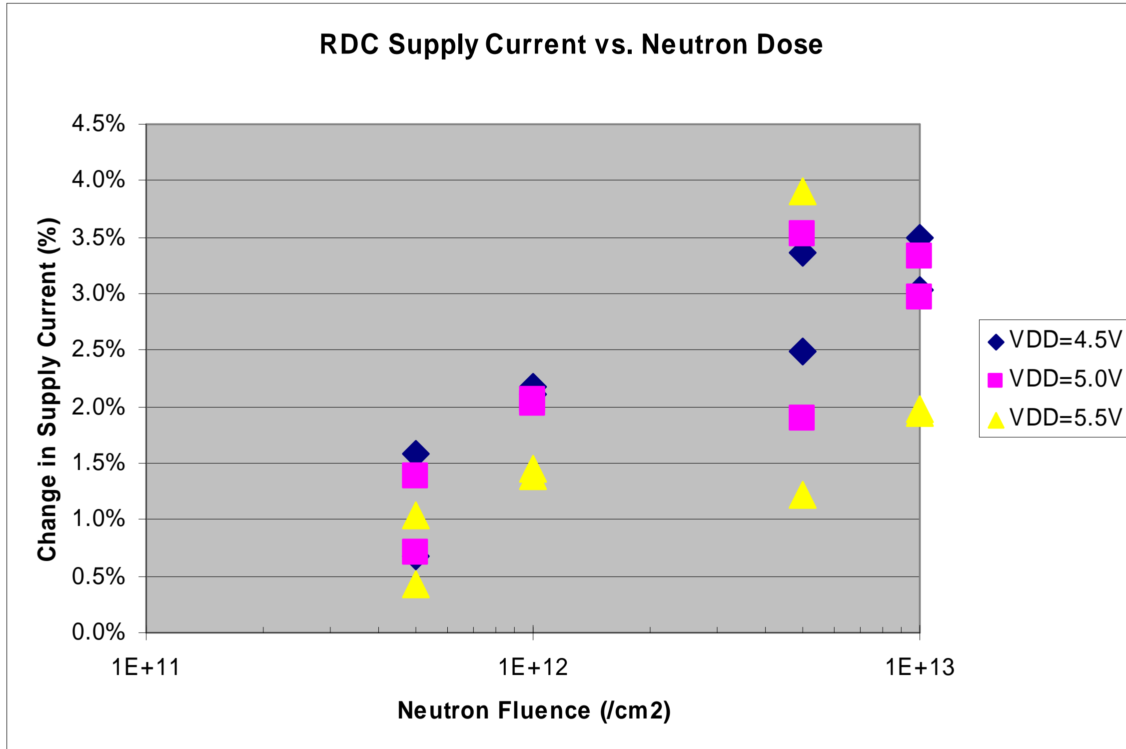

Figure 9. Change in bandgap current with neutron flux.

still latched at elevated temperature). This offers indirect evidence of some bulk displacement damage from the neutrons, since the room-temperature latch-up path is effectively eliminated. It also suggests the possibility that higher neutron fluences might eliminate even the high temperature latch-up susceptibility, but we have no data to confirm this possibility.

Summary

We have shown the current RDC design has a dose-rate-induced latch-up threshold at dose rates around 1e9 rad(Si)/s. This is about one order-of-magnitude too low for many applications. The latch-up results from a pair of long, but adjacent n and p guard rings on a pair of large output transistors. These guard rings were not sufficiently contacted to maintain bias along these long runs. As a result, large photocurrents could easily latch the parasitic PNPN structure where the substrate bias could not be maintained due to resistive losses. The current assets are suitable for applications not having dose-rate requirements, or those having minimum requirements of 1e9 rad(Si)/s. Design modifications (additional substrate guard-ring contacts) have been made to improve the dose-rate latch-up threshold. If levels around 1e10 rad(Si)/s are achieved with these modifications, the RDC should be suitable for most applications.

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