

UTMC Application Note

SμMMIT E & LXE/DXE Built-In-Self-Test Functionality for the JA01 Die

JTAG Instructions:

JTAG defines seven (7) public instructions as follows:

Instruction	Status	UTMC Code msb..lsb	SμMMIT Status
BYPASS	Mandatory	1111 (required all 1's)	Implemented
SAMPLE/PRELOAD	Mandatory	0010	Implemented
EXTEST	Mandatory	0000 (required all 0's)	Implemented
INTEST	Optional	Non-Implemented	N/A
RUNBIST	Optional	Non-Implemented	N/A
IDCODE	Optional	Non-Implemented	N/A
USERCODE	Optional	Not Implemented	N/A

All JTAG operations are determined by the instruction residing in the JTAG instruction register. Instructions are entered into the instruction register by moving through the TAP controller state table with TCK and TMS. Once the SHIFT-IR state is reached, instruction bits are shifted into the TDI. Instructions are shifted LSB to MSB. The last instruction bit is entered when moving from the SHIFT-IR state to the EXIT1-IR state.

Setting the TAP Controller to the TEST-LOGIC-RESET state:

With TCK, TMS, TDI, at logic "1", pulse TRS active low for Xns, or, with TDI, TRS, TMS, at logic "1", clock TCK for 5 rising edges. The TAP controller will now be in the TEST-LOGIC-RESET state.

JTAG Operation of the SμMMIT

JTAG signals:

Inputs: TCK - Test Clock
TMS - Test Mode Select
TDI - Test Data Input
TRS - Test Reset, optional

Output: TDO - Test Data Output

JTAG signal rules:

- TMS is sampled on the rising edge of TCK.
- Change TMS on the falling edge of TCK.
- TDI is sampled on the rising edge of TCK.
- Change TDI on the falling edge of TCK.
- TDO changes on the falling edge of TCK.
(TDO may cross the rising edge of the TCK clock boundary as TCK f_{MAX} increases)
- TMS should be a logic “1” while TRS changes from logic “0” to logic “1”.
- TDO is only ACTIVE when in either SHIFT-IR or SHIFT-DR TAP controller states. For SHIFT-IR, the instruction register is selected to drive TDO. For SHIFT-DR, the test data register is selected to drive TDO.

JTAG elements:

TAP - Test Access Port, includes the JTAG buffers plus drive for global JTAG signals.
JM - JTAG Macro, contains the TAP controller, and the instruction register (IR).
ENREG - Enable Register, holds the scan chain elements for the tri-state control.
BSR - Boundary Scan Register, formed by the abutment of I/O cells.

JTAG TAP controller:

The TAP controller is a synchronous, finite, state machine that responds to changes in TCK and TMS.

The state of the TAP controller determines the state of the input, output, tri-state, and bi-directional buffers, as-well-as the function of TDI and TDO.

For “normal” chip operation, the user should always be in the TEST-LOGIC-RESET state. See the JTAG reset section for methods of selecting this TAP controller state. While the user is “IN” any other state, the instruction controls the state of the I/O buffers.

Instruction operation:

- See the SμMMIT Boundary Scan Register (BSR) order to determine the proper positioning of I/O cells, and the proper number of TCK’s needed to shift in/out the BSR contents.
- Always return to the TEST-LOGIC-RESET state when JTAG operation completes.

SAMPLE/PRELOAD

Objective:

The objective of SAMPLE/PRELOAD is to sample the component inputs or preload the component output data registers.

Method:

From the TEST-LOGIC-RESET state, move to the SHIFT-IR state and apply the SAMPLE/PRELOAD instruction to TDI. Then move to the CAPTURE-DR state. At this time, the inputs are captured and can be shifted out through TDO if the SHIFT-DR state is entered. As captured inputs are shifted out of TDO, the component outputs can be preloaded by applying proper data to TDI. The actual preload occurs when the UPDATE-DR state is entered. Preloading is used before the EXTEST instruction is applied.

The state of the I/O buffers when SAMPLE/PRELOAD is loaded into the IR:

Normal operation.

EXTEST

Objective:

The objective of EXTEST is to drive the component outputs, and to capture the component inputs.

Method:

From the TEST-LOGIC-RESET state, move to the SHIFT-IR state and apply the EXTEST instruction to TDI. Then move to the UPDATE-IR state, at this time the data preloaded into the output data registers are driven to the outputs.

To capture new inputs and drive new outputs, move to the CAPTURE-DR state, at this time the inputs are captured and can be shifted out through TDO if the SHIFT-DR state is entered. As captured inputs are shifted out of TDO, component outputs can be preloaded by applying proper data to TDI. Then move to the UPDATE-DR state, at the next TCK falling edge the outputs will change to the preloaded values. Repeat the above sequences to continue sampling inputs and driving outputs.

The state of the I/O buffers when EXTEST is loaded into the IR:

Inputs operate as normal, outputs are driven with preloaded values, normal system outputs are inhibited from exiting the component as long as EXTEST resides in the instruction register.

BYPASS

Objective:

The objective of BYPASS is to form a connection between TDI and TDO.

Method:

From the TEST-LOGIC-RESET state, move to the SHIFT-IR state and apply the BYPASS instruction to TDI. Then move to the SHIFT-DR state, TDI will now be connected to TDO. The first bit out of TDO will always be a logic "0" followed by bits applied to TDI.

The state of I/O buffers when BYPASS is loaded into the IR:

Normal operation.

S μ MMIT JTAG Boundary Scan Register (BSR) Order

It takes 188 TCK's to shift in/out the entire BSR contents. Of the 188 signals, 83 are inputs, 65 are outputs, and 40 are bidirectional.

There are signals that are not bonded out in the packages, but MUST be considered when shifting data in/out of the BSR. Use the device specific pin list to determine which signals will be available to you.

Position #1 is the first bit which would appear at TDO if the user was shifting out the contents of the BSR.

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
1	ADDRI0	Output
2	RCSB	Output
3	EXI7	Input
4	TCLK	Input
5	DTACKB	Input
6	EXI6	Input
7	YFACKB	Input
8	DA15	Bi-Direct
9	EXI5	Input

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
10	DA14	Bi-Direct
11	EXI4	Input
12	DA13	Bi-Direct
13	MSGACKB	Input
14	BISTB	Output
15	DA12	Bi-Direct
16	DA11	Bi-Direct
17	EC2	Input
18	EC1	Input
19	EXI3	Input
20	EXI2	Input
21	DA10	Bi-Direct
22	EXI1	Input
23	DA9	Bi-Direct
24	EXI0	Input
25	EXISEL	Input
26	DA8	Bi-Direct
27	EC0	Input
28	DA7	Bi-Direct
29	ECS	Output
30	ED7	Input
31	ED6	Input
32	DA6	Bi-Direct
33	ED5	Input
34	DA5	Bi-Direct

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
35	ED4	Input
36	ED3	Input
37	DA4	Bi-Direct
38	ED2	Input
39	DA3	Bi-Direct
40	ED1	Input
41	ED0	Input
42	EA12	Output
43	DA2	Bi-Direct
44	EA11	Output
45	DA1	Bi-Direct
46	EA10	Output
47	DA0	Bi-Direct
48	EA9	Output
49	TMRONAB	Output
50	EA8	Output
51	TAB	Output
52	EA7	Output
53	TA	Output
54	EA6	Output
55	RAB	Input
56	EA5	Output
57	EA4	Output
58	RA	Input
59	EA3	Output

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
60	TMRONBB	Output
61	SASB	Input
62	EXT_SEL	Input
63	TBB	Output
64	EA2	Output
65	TB	Output
66	EA1	Output
67	RBB	Input
68	EA0	Output
69	RB	Input
70	MSEL5	Input
71	NEM	Input
72	TERACB	Output
73	MSEL4	Input
74	READYB	Output
75	MSEL3	Input
76	PC11	Output
77	MSEL2	Input
78	SSYSFB	Input
79	PC10	Output
80	RTA4	Input
81	PC9	Output
82	RTA3	Input
83	PC8	Output
84	RTA2	Input

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
85	PC7	Output
86	IDATA7	Input
87	PC6	Output
88	IDATA6	Input
89	RTA1	Input
90	IDATA5	Input
91	RTA0	Input
92	IDATA4	Input
93	RTPTY	Input
94	IDATA3	Input
95	LOCKB	Input
96	ABBSTD	Input
97	IDATA2	Input
98	PC5	Output
99	IDATA1	Input
100	PC4	Output
101	IDATA0	Input
102	MSEL1	Input
103	PC3	Output
104	MSEL0	Input
105	PC2	Output
106	MRSTB	Input
107	RDYB	Output
108	PC1	Output
109	RDB	Input

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
110	PC0	Output
111	DSB	Input
112	TRSTN	Input
113	TDO	Output
114	TDI	Input
115	TMS	Input
116	TCK	Input
117	ALE	Input
118	PCK	Output
119	DMARB	Output
120	EXI31	Input
121	DMAGB	Input
122	EXI30	Input
123	EMOEB	Output
124	EMCS1B	Output
125	EMWRB	Output
126	DMACKB	Output
127	MSG_INTB	Output
128	EXI29	Input
129	YF_INTB	Output
130	EXI28	Input
131	AUTOENB	Input
132	EXI27	Input
133	EXI26	Input
134	EXI25	Input

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
135	ADDRI15	Output
136	EXI24	Input
137	ROMEN	Output
138	ADDRI14	Output
139	CSB	Input
140	ADDRI13	Output
141	RD_WRB	Input
142	ADDRESS15	Bi-Direct*
143	EXI23	Input
144	ADDRESS14	Bi-Direct*
145	EXI22	Input
146	ADDRESS13	Bi-Direct*
147	ADDRI12	Output
148	EXI21	Input
149	ADDRESS12	Bi-Direct*
150	EXI20	Input
151	ADDRESS11	Bi-Direct*
152	EXI19	Input
153	ADDRESS10	Bi-Direct*
154	EXI18	Input
155	ADDRI11	Output
156	ADDRESS9	Bi-Direct*
157	ADDRI10	Output
158	ADDRESS8	Bi-Direct*
159	ADDRI9	Output

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
160	ADDRI8	Output
161	EXI17	Input
162	ADDRESS7	Bi-Direct*
163	EXI16	Input
164	MHZ24	Input
165	EXI15	Input
166	ADDRI7	Output
167	EXI14	Input
168	ADDRESS6	Bi-Direct*
169	EXI13	Input
170	ADDRESS5	Bi-Direct*
171	EXI12	Input
172	ADDRI6	Output
173	ADDRI5	Output
174	ADDRESS4	Bi-Direct
175	ADDRI4	Output
176	ADDRESS3	Bi-Direct
177	ADDRI3	Output
178	EXI11	Input
179	ADDRESS2	Bi-Direct
180	EXI10	Input
181	ADDRESS1	Bi-Direct
182	ADDRI2	Output
183	EXI9	Input
184	ADDRI1	Output

Table 1: S μ MMIT JTAG BSR Order

Position	Name	BSR Type
185	ADDRESS0	Bi-Direct
186	EXI8	Input
187	RWRB	Output
188	RRDB	Output

* The Address[15:5] are bi-directional for the NON-RadHard S μ MMIT and S μ MMIT LXE/DXE product, and are output only for the RadHard version of the JA01 die.