

Aeroflex Colorado Springs Application Note

Noise Analysis for Simultaneously Switching Outputs on the UT6325 RadHard Eclipse FPGA

Introduction

As FPGA technology evolves, designs continue to grow in terms of both total pin count and active bus width. I/O buffer design is also changing to meet a need for increased current source / sink capability and faster switching edge rates. This combination of factors results in an increase in ground bounce or noise caused by simultaneously switching outputs (SSOs) in the FPGA design. The noise can affect device reliability since it can trigger false edges on critical input signals.

For example, the UT6325 RadHard Eclipse has I/O buffers designed to support GTL+ and SSTL2 interfaces requiring 24mA current source or sink. The switching edge rates for these buffers are very fast, typically 2.8 V/ns for fast slew rate buffers and 1.0 V/ns for slow slew rate buffers. The noise generated by these fast switching currents needs to be characterized to evaluate the affects on both bidirectional I/O pins and the special input only pins used for clock and high drive control signals in the RadHard Eclipse. The high drive, input only signals are especially at issue, since these signals are all LVCMOS2 type inputs. The LVCMOS2 inputs are referenced to the 2.5V, Vcc core voltage supply. The bidirectional I/O are referenced to the 3.3V Vccio I/O power supplies.

The initial SSO noise analysis on the UT6325 RadHard Eclipse in a 208 CQFP package. Future noise analysis will be done on the 288 CQFP and 484 CLGA packages.

UT6325 Noise Test Circuit

In order to evaluate SSO noise in the UT6325 (208 CQFP package), a special test circuit was created with 64 toggle flops controlled by 13 separate enable lines. The first enable tri-states the outputs from 16 toggle flops. The remaining 12 enable lines each control the tri-state output of 4 additional toggle flops. This allows Aeroflex to observe the effects of incremental noise by adding groups of 4 toggle flops to the initial 16. The first bank of 16 toggle flop outputs is placed in one corner and side of the die, as far away from any ground and power pins as possible. Each succeeding set of 4 toggle flop outputs is placed on one or the other side of the initial bus of 16. In this manner, all 13 banks for toggle flop outputs are placed. The toggle flop outputs are physically placed as close together as possible, skipping only power, ground or input only pins during placement.

To observe the effects of SSO noise, 16 additional toggle flops are used. Each toggle flop is initially preset high. A noise sensitive input is connected to the clear pin for each toggle flop. The input to the clear is held low on the tester. The test looks for sufficient noise from SSOs to cause a ground bounce glitch on the critical input which then clears the toggle flop. Sixteen flops are used in order to observe all types of possible inputs. Four critical inputs use global and quadrant clock resources. Four critical inputs use standard TTL/CMOS input pads. The final 8 inputs use the high drive input only signals

found imbedded in each of the 8 I/O banks. Each critical input is placed within the busses of SSOs, as far away from power and ground pins as is possible.

The above noise design is implemented in two ways to evaluate noise. The first circuit uses the fast slew switching outputs for all toggle flops. The second circuit uses the slow slew switching outputs for all toggle flops.

Noise Test on the Trillium Tiger

The Tiger tester is used to evaluate the noise design. Tester output loading for each I/O on the DUT is evaluated with constant dc current loads of 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 22, and 24mA. The Tiger attempts to pull each pin on the UT6325 to a mid-level voltage, while the DUT sources or sinks dc current as necessary. The V_{il} offset on the Tiger is evaluated at 0, 100, 200, 300, 400 and 500mV, in order to raise the ground plane and lower noise margin. The core voltage on the DUT is varied from 2.1V to 2.8V in increments of 100mV. The I/O voltage is evaluated from 2.8V to 3.8V, again in increments of 100mV. These wide ranges for the core and I/O voltage are defined to evaluate the UT6325 device well beyond its' normal operating range. Nominal operating voltage for the UT6325 is a V_{cc} core voltage of 2.5V and a V_{ccio} I/O voltage of 3.3V. The maximum operating voltage range for the core of the UT6325 is 2.3V to 2.7V. The maximum operating voltage range for the V_{ccio} I/O supply is 3.0V to 3.6V. This full test is run on multiple units programmed with both fast slew rate and slow slew rate buffers.

Noise Test Results using Slow Slew Output Buffers

Test results for devices with slow slew output buffers are summarized in the following 3 tables.

Device Number	(All)
Output Load (mA)	24
Vil Offset	0MV

		Core Voltage (V)							
Data	I/O Voltage (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8
Average of Number Of Switching Outputs	2.8								
	2.9								
	3								
	3.1								
	3.2								
	3.3								
	3.4								
	3.5								
	3.6								
	3.7								
3.8									

Table 1: Slow Slew Output Buffers with 24mA Output Load and 0V offset

Table 1 shows results for the UT6325 under good grounding conditions. Even when the DUT sources or sinks 24mA of dc current, not enough SSO noise occurs to cause an input error. All 60 possible SSO are used in this test, and the Tiger tester cycles on this vector set for several thousand cycles evaluating the test.

Device Number	(All)
Output Load (mA)	12
Vil Offset	300mV

		Core Voltage (V)								
Data	I/O Voltage (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	
Average of Number Of Switching Outputs	2.8	48	56							
	2.9	46	56	64						
	3	44	54	60						
	3.1	42	50	58						
	3.2	38	46	56						
	3.3	36	44	54						
	3.4	36	40	48	62					
	3.5	30	36	44	54					
	3.6	28	34	40	50	62				
	3.7	28	30	36	44	54				
	3.8	60							30	
Average of Gnd Bounce Per Switching Output	2.8	0.017	0.015							
	2.9	0.018	0.015	0.014						
	3	0.018	0.016	0.015						
	3.1	0.019	0.017	0.015						
	3.2	0.021	0.019	0.016						
	3.3	0.023	0.019	0.017						
	3.4	0.023	0.022	0.019	0.015					
	3.5	0.027	0.024	0.020	0.017					
	3.6	0.029	0.025	0.023	0.019	0.016				
	3.7	0.029	0.029	0.025	0.021	0.018				
	3.8	0.014							0.036	

Table 2: Slow Slew Output Buffers with 12mA Output Load and 300mV Ground Offset

Table 2 shows the effect of poor grounding. In this test, 300mV of ground offset is applied to each DUT. Failures can be seen, with various conditions of core voltage, I/O voltage and SSOs. To read data from the top section of the table, each entry identifies the number of SSOs necessary to cause a failure for a given core and I/O voltage combination. The Tiger tester also logs which output caused this first failure.

Under maximum recommended operation conditions, the worst case number of SSOs necessary to cause failure was 40. This occurred at the point of minimum core voltage (2.3V), and maximum I/O voltage (3.6V). The first failures, as logged by the Tiger, occur on the LVCMOS2 input only pins. Specifically, the global clock and high drive input embedded in the first group of 16 SSOs. This was our worst case placement of LVCMOS2 inputs, farthest from ground pins and surrounded by all banks of SSOs.

The second section of the table identifies the amount of ground bounce, in volts, recorded for each SSO when a failure condition occurs. For the failure identified above, 0.023V (230mV) of ground bounce was created by each of the 40 SSOs.

Device Number	(All)
Output Load (mA)	(All)
Vil Offset	(All)

		Core Voltage (V)								
Data	I/O Voltage (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	
Average of Number Of Switching Outputs	2.8	26	28	27	28	31	30	31	34	
	2.9	26	28	28	28	31	30	31	34	
	3	25	28	28	27	30	30	30	34	
	3.1	24	26	28	27	30	31	30	33	
	3.2	24	25	28	27	29	32	29	33	
	3.3	24	24	27	26	28	31	30	32	
	3.4	24	24	26	27	28	30	30	32	
	3.5	23	24	25	26	28	29	31	31	
	3.6	23	24	25	26	27	29	31	31	
	3.7	22	23	24	25	26	28	30	31	
3.8	29	27	29	32	30	33	36	27		
	(blank)									
Average Bounce Per Switching Output	2.8	0.034	0.034	0.036	0.036	0.035	0.038	0.037	0.036	
	2.9	0.035	0.035	0.036	0.037	0.036	0.037	0.037	0.036	
	3	0.036	0.035	0.036	0.037	0.036	0.038	0.038	0.037	
	3.1	0.037	0.036	0.036	0.038	0.037	0.037	0.038	0.037	
	3.2	0.038	0.038	0.036	0.038	0.038	0.036	0.039	0.038	
	3.3	0.038	0.039	0.038	0.039	0.038	0.037	0.039	0.038	
	3.4	0.039	0.039	0.039	0.038	0.039	0.038	0.038	0.038	
	3.5	0.039	0.040	0.040	0.040	0.039	0.039	0.039	0.039	
	3.6	0.040	0.040	0.040	0.040	0.040	0.040	0.039	0.039	
	3.7	0.041	0.041	0.041	0.041	0.041	0.041	0.040	0.040	
3.8	0.032	0.034	0.034	0.034	0.036	0.035	0.034	0.046		

Table 3: Average Results for all Slow Slew Output Buffers under all Conditions

Table 3 shows results for all devices tested across all test conditions. In general, the failures identified occur with 500mV of ground offset, and 20 – 24mA of output load current. The exact worst case load current varies slightly, depending on core and I/O voltage conditions. Please note from the table that even under these extreme conditions, the DUT switches 24 slow slew rate buffers throughout the maximum recommended voltage operating range without failure.

Noise Test Results using Fast Slew Output Buffers

Test results for the UT6325 device with fast slew output buffers show a reduction in the noise margin due to SSOs. These results are summarized in the following 3 tables.

Device Number	(All)
Output Load (mA)	8
Vil Offset	0mV

		Core Voltage (V)							
Data	I/O Voltage (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8
Average of Number Of Switching Outputs	2.8								
	2.9								
	3								
	3.1								
	3.2								
	3.3								
	3.4								
	3.5		36						
	3.6		32	36					
Average of Gnd Bounce Per Switching Output	2.8								
	2.9								
	3								
	3.1								
	3.2								
	3.3								
	3.4								
	3.5		0.023						
	3.6		0.026	0.024					
3.7		0.041	0.033	0.020					
3.8		0.041	0.043	0.037					

Table 4: Fast Slew Output Buffers with 8mA Output Load and 0V offset

Table 4 shows test results for the fast slew rate buffers. The data in the tables is interpreted as before, with the first section for each condition identifying the number of SSO necessary to cause a failure and the second section showing the ground bounce per switching output during that failure. With good grounding of 0mV offset and 8mA of dc load on the SSOs, the DUT is beginning to show errors. Notice that the error conditions are outside of the maximum operating conditions for the UT6325. Regardless, table 4 shows the effect of the fast slew rate buffers for SSO noise, with 44 and 36 SSO buffers causing failure just outside of these maximum conditions. The same LVCMOS2 inputs which failed during the slow slew rate test are the first buffers to fail here.

Device Number	(All)
Output Load (mA)	8
Vil Offset	300mV

		Core Voltage (V)							
Data	I/O Voltage (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8
Average of Number Of Switching Outputs	2.8	20	20	20	20	20	20	24	48
	2.9	20	20	20	20	20	20	20	24
	3	20	20	20	20	20	20	20	20
	3.1	20	20	20	20	20	20	20	20
	3.2	20	20	20	20	20	20	20	20
	3.3	20	20	20	20	20	20	20	20
	3.4	20	20	20	20	20	20	20	20
	3.5	16	20	20	20	20	20	20	20
	3.6	16	16	20	20	20	20	20	20
	3.7	16	16	20	20	20	20	20	20
3.8	20	20	20	20	24	44		20	
Average of Gnd Bounce Per Switching Output	2.8	0.041	0.043	0.045	0.047	0.049	0.051	0.044	0.023
	2.9	0.041	0.043	0.045	0.047	0.049	0.050	0.052	0.045
	3	0.041	0.043	0.045	0.047	0.049	0.050	0.053	0.054
	3.1	0.041	0.043	0.045	0.047	0.049	0.050	0.052	0.055
	3.2	0.041	0.043	0.045	0.047	0.049	0.050	0.052	0.054
	3.3	0.041	0.043	0.045	0.047	0.048	0.050	0.052	0.054
	3.4	0.041	0.043	0.045	0.047	0.049	0.050	0.052	0.054
	3.5	0.051	0.043	0.045	0.047	0.049	0.050	0.052	0.054
	3.6	0.051	0.053	0.045	0.047	0.049	0.051	0.052	0.054
	3.7	0.051	0.053	0.045	0.046	0.049	0.051	0.052	0.054
3.8	0.041	0.043	0.045	0.047	0.040	0.023		0.054	

Table 5: Fast Slew Output Buffers with 8mA Output Load and 300mV Ground Offset

Table 5 again shows the effect of poor grounding in the SSO test. Poor grounding exerts an even greater effect for fast slew rate buffers. In this test, the Tiger applies 300mV of ground offset. With 2mA of current load, as few as 20 SSO cause enough noise to generate an input failure for tests throughout the voltage operating region.

Device Number	(All)
Output Load (mA)	(All)
Vil Offset	(All)

		Core Voltage (V)								
Data	I/O Voltage (V)	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	
Average of Number Of Switching Outputs	2.8	19	20	20	22	22	23	23	24	
	2.9	19	19	20	21	22	22	23	23	
	3	19	19	20	20	20	21	22	22	
	3.1	19	19	19	20	20	21	21	22	
	3.2	18	19	19	19	19	20	21	21	
	3.3	18	18	19	19	19	20	20	21	
	3.4	18	18	18	19	19	19	20	21	
	3.5	18	18	18	18	19	19	19	20	
	3.6	18	18	18	18	18	19	19	20	
	3.7	18	18	18	18	18	19	19	19	
	3.8	20	21	21	22	22	23	24	19	
	(blank)									
Average of Gnd Bounce Per Switching Output	2.8	0.043	0.045	0.046	0.046	0.047	0.047	0.049	0.049	
	2.9	0.044	0.045	0.047	0.048	0.048	0.049	0.049	0.050	
	3	0.045	0.046	0.047	0.049	0.049	0.050	0.051	0.051	
	3.1	0.045	0.047	0.048	0.049	0.050	0.051	0.052	0.052	
	3.2	0.045	0.047	0.048	0.050	0.051	0.052	0.052	0.054	
	3.3	0.045	0.047	0.049	0.050	0.051	0.053	0.053	0.054	
	3.4	0.046	0.048	0.050	0.051	0.052	0.054	0.054	0.055	
	3.5	0.046	0.048	0.050	0.052	0.052	0.054	0.055	0.055	
	3.6	0.046	0.048	0.050	0.052	0.053	0.054	0.056	0.057	
	3.7	0.047	0.049	0.050	0.052	0.054	0.055	0.056	0.058	
	3.8	0.042	0.043	0.044	0.045	0.046	0.047	0.048	0.058	

Table 6: Average Results for all Fast Slew Output Buffers under all Conditions

Table 6 summarizes results for the fast slew rate buffers across all test conditions. As before, the worst case test conditions are where 500mV of ground offset are applied and very high current load is applied to each output on the DUT. Reviewing the table shows that under minimum core and maximum I/O voltage conditions, as few as 18 SSO could cause a failure. Compare this to the summarized results for slow slew rate buffers where 24 SSO were able to switch without failure.

Summary

In summary, noise due to SSOs using the slow slew rate I/O buffers is not a major concern for the UT6325 FPGA in the 208 CQFP package. The user must maintain the core and I/O voltages within their maximum operating range, provide a solid ground with limited offset, and limit the current source / sink requirements on the device. Only under extreme conditions were failures identified. No failures ever occurred on a bidirectional LVCMOS3 pin. Only the input only, LVCMOS2 pins showed failures.

SSO noise due to the fast slew rate I/O buffers is a concern. The designer should limit his use of this buffer type, reserving it for those few instances where speed is of greatest concern. When fast slew rate buffers are used, the designer should also attempt to distribute the buffers around the 8 separate banks allowed on the UT6325. Minimize usage within any bank which contains a critical LVCMOS2 input. Where possible, the fast slew rate buffers should be placed near Vccio and GND pins. Critical LVCMOS2 input signals should then be physically placed as far away as possible from fast slew rate SSOs.