

UTMC APPLICATION NOTE

UT69R000 Bus Control

Data Transfer Acknowledge ($\overline{\text{DTACK}}$) Operation

The 69R000 allows the user to insert wait states into read and write cycles performed on the operand bus. As long as Data Transfer Acknowledge ($\overline{\text{DTACK}}$) is high the bus cycle stretches. The cycle continues to hold until the $\overline{\text{DTACK}}$ goes low and either Bus Error ($\overline{\text{BTERR}}$) or Memory Protect (MPROT) become active. MPROT is active high; therefore, the user must ground $\overline{\text{MPROT}}$ or use control circuitry. If a condition occurs that causes MPROT to float, it could cause $\overline{\text{DTACK}}$ to be ignored.

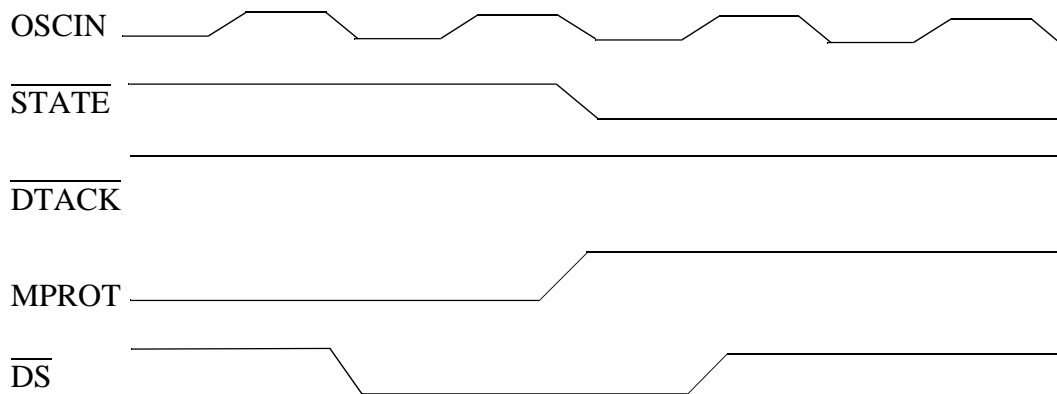


Figure 1. $\overline{\text{DTACK}}$ Cycle MPROT High

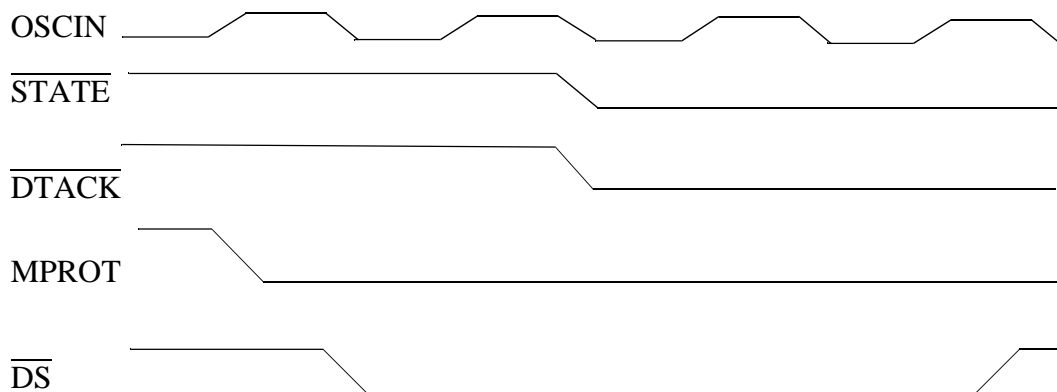


Figure 2. $\overline{\text{DTACK}}$ Cycle MPROT Low